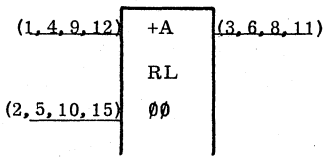
TX01 TAPE CONTROLLER HANDOUT

INTRODUCTION

This section provides basic logic information pertaining to the individual components used on circuit cards of the Control Unit. Each block shows the input pins on the left and the output pins on the right. A description of each circuit function is provided, and the voltage and ground pins are identified. The blocks are listed in numerical order.

SN 7400

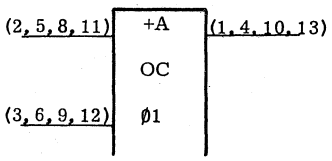


2-Input, + NAND (4/Chip)

+ on input Pins 1 and 2 produces - on output Pin 3.
- on either or both inputs causes Pin 3 to be +.

+5 on Pin 14
GND on Pin 7

SN 7401

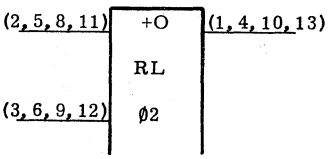


2-Input, + NAND (4/Chip)
Open Collector output

+ on input Pins 2 and 3 produces - on output Pin 1.
- on either or both inputs causes Pin 1 to be +

+5 on Pin 14
GND on Pin 7

SN 7402

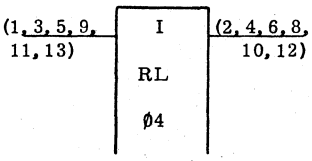


2-Input, + NOR (4/Chip)

+ Signal on input Pins 2 and/or 3 results in a negative (-) output on Pin 1.

+5 on Pin 14
GND on Pin 7

SN 7404

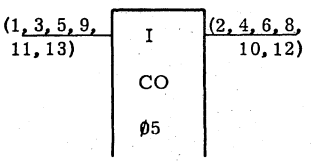


Hex Inverter (6/Chip)

+ on Pin 1 results in a - on Pin 2
- on Pin 1 results in a + on Pin 2

+5 on Pin 14
GND on Pin 7

SN 7405

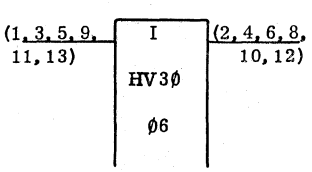


Hex Inverter (6/Chip)
Open Collector output

+ on Pin 1 results in a - on Pin 2
- on Pin 1 results in a + on Pin 2

+5 on Pin 14
GND on Pin 7

SN 7406

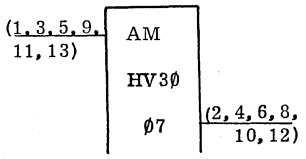


Hex Inverter (6/Chip)
High Voltage

+ on Pin 1 results in a - on Pin 2
- on Pin 1 results in a + on Pin 2

+5 on Pin 14
GND on Pin 7

SN 7407



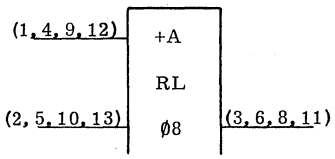
Hex Buffer (6/Chip)
High Voltage

+ on Pin 1 results in a + on Pin 2.
- on Pin 1 results in a - on Pin 2.

Voltage level on output pins:
- up to 30V.

+5 on Pin 14
GND on Pin 7

SN 7408

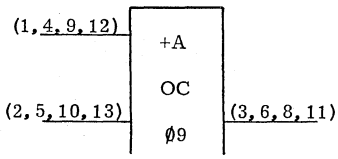


2-Input, + AND (4/Chip)

+ on input Pins 1 and 2 results in a + on output Pin 3 .
- on either or both input Pins 1 and 2 results in a - on output Pin 3.

+5 on Pin 14
GND on Pin 7

SN 7409

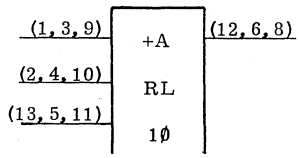


2-Input, + AND (4/Chip)
Open Collector

+ on input Pins 1 and 2 results in a + on output Pin 3.
- on either or both input Pins 1 and 2 results in a - on output Pin 3.

+5 on Pin 14
GND on Pin 7

SN 7410

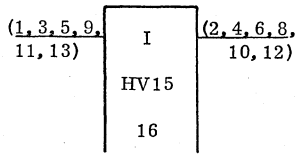


3-Input, + NAND (3/Chip)

+ on input Pins 1, 2 and 13 results in a - on output Pin 12.
- on any or all input Pins 1, 2, and 13 results in a + on output Pin 12.

+5 on Pin 14
GND on Pin 7

SN 7416

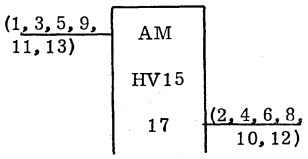


Hex Inverter (6/Chip)
High Voltage

+ on input Pin 1 results in a - on output Pin 2.
- on input Pin 1 results in a + on output Pin 2.

+5 on Pin 14
GND on Pin 7

SN 7417

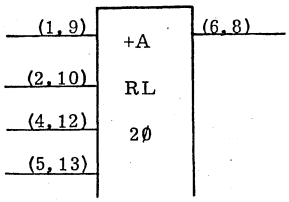


Hex Inverter (6/Chip)
High Voltage

+ on input Pin 1 results in a + on output Pin 2.
- on input Pin 1 results in a - on output Pin 2.

+5 on Pin 14
GND on Pin 7

SN 7420

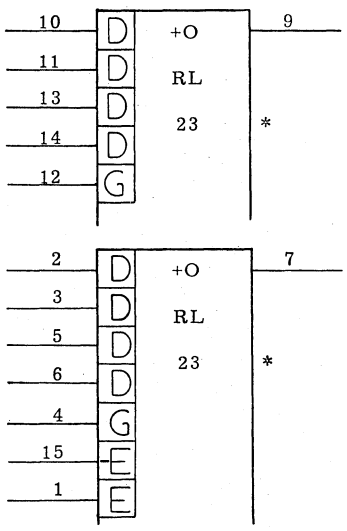


4-Input, + NAND (2/Chip)

+ on input Pins 1, 2, 4 and 5 results in a - on output Pin 6.
- on any or all input Pins 1, 2, 4 and 5 results in a + on output Pin 6.

+5 on Pin 14
GND on Pin 7

SN 7423

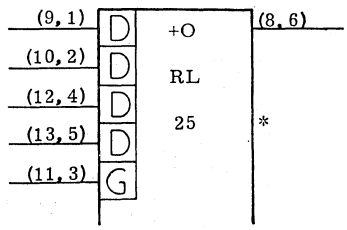


4-Way Gated OR Extender

The 4-Way Gated OR chip is described for RL25 below.
The extender function does not require Pin 4 gating. When Pin 15 is - and Pin 1 is +, Pin 7 will be minus.

+5 on Pin 16
GND on Pin 8

SN 7425

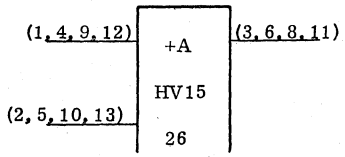


4-Way Gated OR (2/Chip)

Output Pin 8 will be minus if input Pin 11 (gate) is plus and a plus is present on Pins 9, 10, 12 or 13

+5 on Pin 14
GND on Pin 7

SN 7426

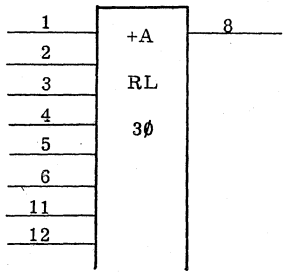


2-Input, + NAND (4/chip)
High Voltage Output

+ on input Pins 1 and 2 results in a - on the output Pin 3.
- on either or both inputs causes Pin 3 to be +.

+5 on Pin 14
GND on Pin 7

SN 7430

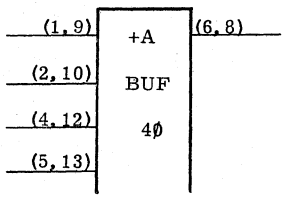


8-Input, + NAND (1/chip)

+ on all input pins results in a - on Pin 8.
- on any or all input pins causes Pin 8 to be +.

+5 on Pin 14
GND on Pin 7

SN 7440

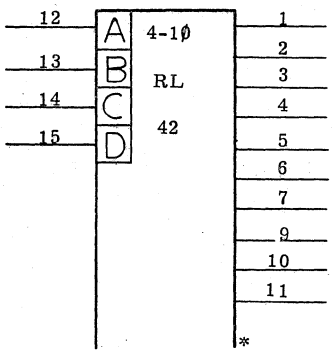


4-Input, + NAND (2/chip)

+ on input Pins 1, 2, 4 and 5 results in - on Pin 6.
- on any or all input pins results in + on output Pin 6.

+5 on Pin 14
GND on Pin 7

SN 7442

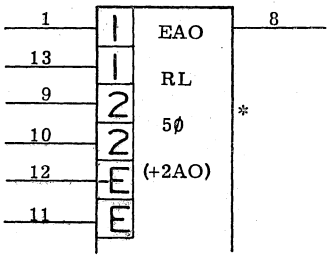


4 to 10 Decoder

PIN				"-" on Pin	Binary Value
12	13	14	15		
-	-	-	-	1	0
-	-	-	+	2	1
-	-	+	-	3	2
-	-	+	+	4	3
-	+	-	-	5	4
-	+	-	+	6	5
-	+	+	-	7	6
-	+	+	+	9	7
+	-	-	-	10	8
+	-	-	+	11	9

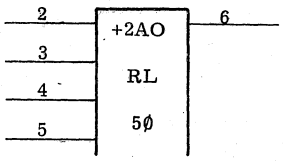
+5 on Pin 16
GND on Pin 8

SN 7450



Expandable 2-Input AND/OR Invert

Output Pin 8 will be minus if:
1. Input Pins 1 and 13 are +.
2. Input Pins 9 and 10 are +.
3. Input Pin 12 is -, and Pin 13 is +.

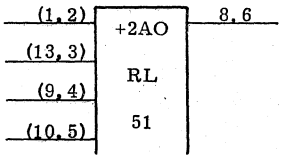


Output Pin 6 will be minus if:

1. Input Pins 2 and 3 are plus.
2. Input Pins 4 and 5 are plus.

+5 on Pin 14
GND on Pin 7

SN 7451



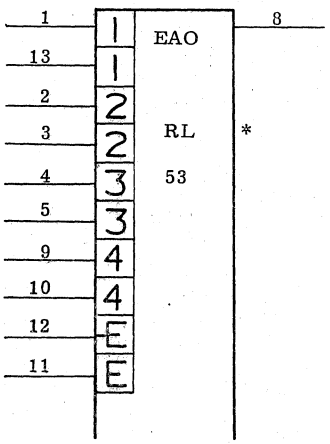
2-Input AND/OR Invert (2/chip)

Output Pin 8 will be minus if:

1. Input Pins 1 and 13 are plus.
2. Input Pins 9 and 10 are plus.

+5 on Pin 14
GND on Pin 7

SN 7453

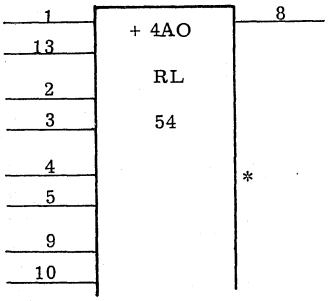


Expandable 4-Wide, 2-Input AND/OR Invert

Output Pin 8 will be minus if:

1. Input Pins 1 and 13 are plus.
2. Input Pins 2 and 3 are plus.
3. Input Pins 4 and 5 are plus.
4. Input Pins 9 and 10 are plus.
5. Input Pin 12 is minus and Pin 11 is plus.

SN 7454

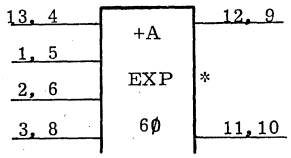


2-Input, 4-wide, AND/OR Invert

Output Pin 8 will be minus if:
1. Pins 1 and 13 are plus.
2. Pins 2 and 3 are plus.
3. Pins 4 and 5 are plus.
4. Pins 9 and 10 are plus.

+5 on Pin 14
GND on Pin 7

SN 7460

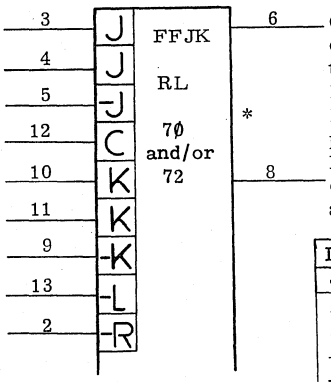


4-Input Dual Expander (2/chip)

Output Pin 12 will be minus and Pin 11 will be plus when input Pins 13, 1, 2 and 3 are all plus.

+5 on Pin 14
GND on Pin 7

SN 7470 & 7472



Edge Trigger JK Flip-Flop
JK Master-Slave Flip-Flop

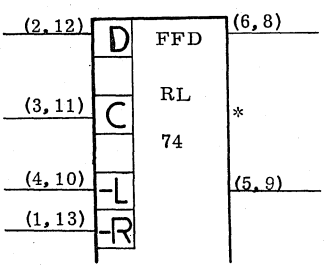
Outputs flip on positive edge of clock pulse as indicated in the table. Minus on input Pin 13 (-L) causes output Pin 6 to go positive and output Pin 8 to go negative. Minus on input Pin 2 (-R) causes Pin 6 to go negative and Pin 8 to go positive.

Input		Output	
J	K	8**	6**
-	-	No effect	
-	+	-	+
+	-	+	-
+	+	Complements	

** J is + on Pins 3 and 4, - on 5
K is + on Pins 10 and 11, - on 9 } RL70

J is + on Pins 3, 4 and 5
K is + on Pins 9, 10 and 11 } RL72

SN 7474



Dual D-Type Edge Trigger Flip-Flop (2/chip)

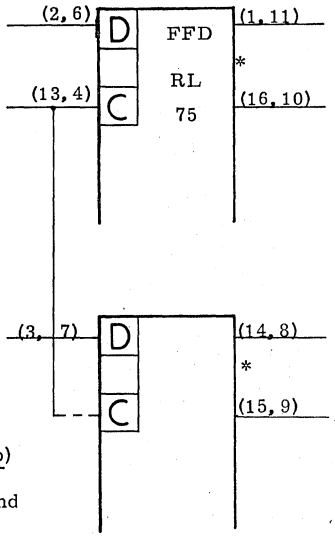
Level on Pin 2, at clock pulse time (Pin 3), is gated to Pin 5; Pin 6 is inverted. This level is maintained until the next clock pulse.

The -L input on Pin 4 causes Pin 5 to go positive without a clock pulse.

The -R input on Pin 1 causes Pin 5 to go negative without a clock pulse.

+5 on Pin 14
GND on Pin 7

SN 7475

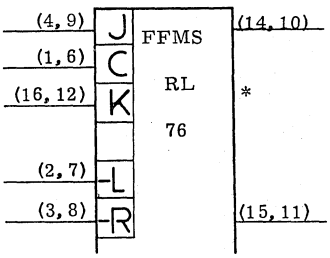


Quad D Edge Trigger Flip-Flop

Level on the D input at clock (C input) time is gated to Pin 16 and maintained until the next clock pulse. Pin 1 is inverted output. The chip has only two clock inputs, so two flip-flops use the same clock pulse.

+5 on Pin 5
GND on Pin 12

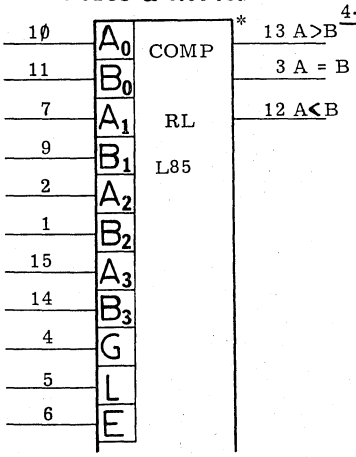
SN 7476



Dual JK Master-Slave Flip-Flop (2/chip)

Outputs flip on positive edge of clock pulse (Pin 1). Minus on input Pin 2 (-L) causes output Pin 14 to go positive and Pin 15 to go negative. Minus on input Pin 3 (-R) causes Pin 14 to go negative and Pin 15 to go positive. Reference truth table for RL72.
+5 on Pin 5
GND on Pin 13

SN 74L85 & SN7485



4-Bit Magnitude Comparator

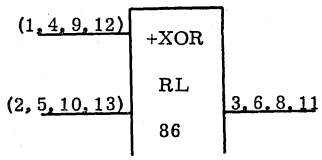
The three outputs can be fed into another comparator on the G, L and E (greater, lesser, equal) inputs

+5 on Pin 16
GND on Pin 8

Inputs								Output
A3 B3	A2 B2	A1 B1	Ao Bo	G	L	E		+ on Pin
+ -								A > B
- +								A < B
Same	+ -							A > B
Same	- +							A < B
Same	Same	+ -						A > B
Same	Same	- +						A < B
Same	Same	Same	+ -					A > B
Same	Same	Same	- +					A < B
Same	Same	Same	Same	+	-	-		A > B
Same	Same	Same	Same	-	+	-		A < B
Same	Same	Same	Same	-	-	+		A=B

Same indicates that both are plus or both are minus.

SN 7486

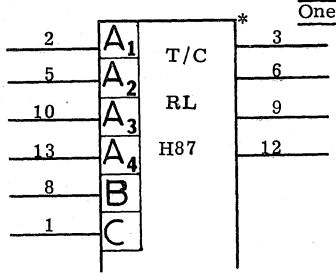


2-Input Exclusive OR (4/chip)

Output Pin 3 will be plus if either (not both) input Pins 1 or 2 are plus.

+5 on Pin 14
GND on Pin 7

SN 74H87

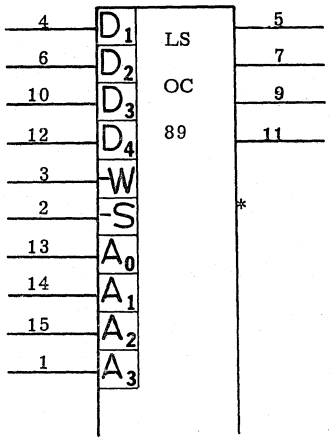


4-Bit True Complement Zero One Bit

Input		Output			
8	1	3	6	9	12
-	-	2	5	10	13
-	+	2	5	10	13
+	-	+	+	+	+
+	+	-	-	-	-

+5 On Pin 14
GND on Pin 7

SN 7489

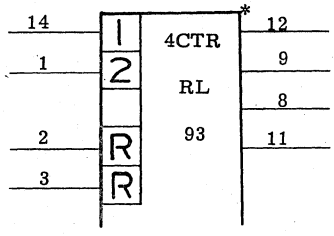


64-Bit R/W Memory

Pins 4, 6, 10 and 12 are data inputs. Each input can be gated into 16 different 'cells', if Pin 3 is minus. Input pins 1, 15, 14 and 13 determine the 'cell' into which data is 'written', or gated out. Data will be gated out (read) if Pin 2 is minus.

+5 on Pin 16
GND on Pin 8

SN 7493



4-Bit Binary Counter

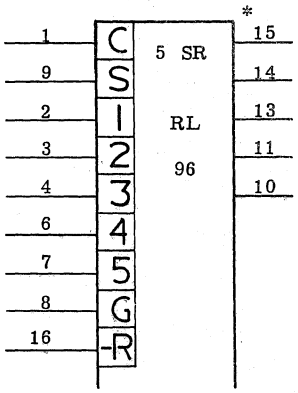
Output Pin 12 is normally connected to Pin 1. Both R inputs must be plus to reset the counter. Either or both R inputs minus allows the counter to count. Counter increments once per pulse on Pin 14. The outputs have the following binary values:

12 = 1
9 = 2
8 = 4
11 = 8

Example: If counter equals 9, outputs 11 and 12 would be positive.

+5 on Pin 5
GND on Pin 10

SN 7496

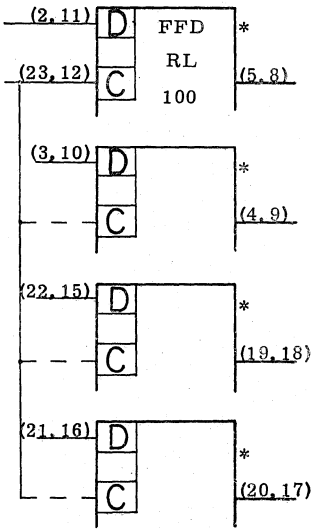


5-Bit Shift Register

The output on Pin 15 will follow input Pin 9 if a clock pulse is present at input 1. The next clock pulse will shift the output at Pin 15 to Pin 14 and Pin 15 will follow the 9 input. Data continues to shift (15 to 14, 14 to 13, 13 to 11, and 11 to 10) with every clock pulse. Outputs 15 thru 10 can also be set or reset by a + on input Pin 8. Then output Pin 15 will follow input Pin 2. (Pin 14 follows Pin 3, etc) while the Pin 8 input is plus. A minus on Pin 16 resets the shift register and outputs 15 thru 10 will be minus.

+5 on Pin 5
GND on Pin 12

SN 74100



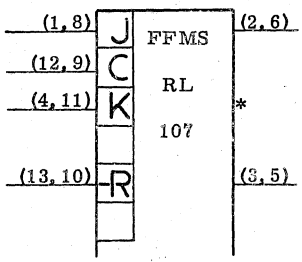
Dual Quad D-Type Edge Trigger Flip-Flop

Level on D input at clock (C) time is gated to Pin 5 and maintained until the next clock pulse.

Four flip-flop circuits share the same clock pulse.

+5 on Pin 24
GND on Pin 7

SN 74107



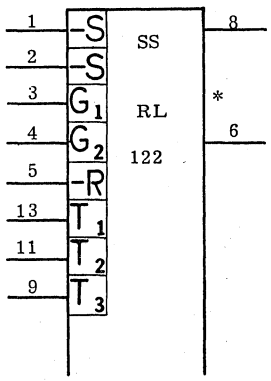
Dual JK Master-Slave Flip-Flop

Outputs flip on positive edge of clock pulse (Pin 12). Minus on input Pin 13 (-R) causes Pin 2 to go negative and Pin 3 to go positive.

Input		Output	
J	K	3	2
-	-	No effect	
-	+	-	+
+	-	+	-
+	+	Complements	

+5 on Pin 14
GND on Pin 7

SN 74122



Single Shot

Inputs T_1, T_2, and T_3 are used for external RC networks to increase the time of the single shot. When a minus is present on the -R input it causes output Pin 8 to go negative and output Pin 6 to go positive.

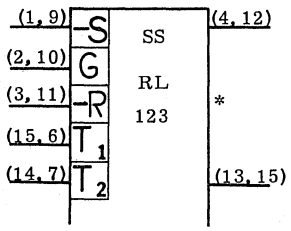
Vcc on pin 14,
GND on pin 7

Input		Output	
-S	G	8	6
+	x	-	+
x	-	-	+
↓	↑	⎍	⎎

Code: x = + or -
↓ = + to - transition
↑ = - to + transition

Input Pins				Output Pins	
1	2	3	4	8	6
+	+	x	x	-	+
x	x	-	+	-	+
x	x	x	-	-	+
-	x	+	+	-	+
-	x	↑	+	⎍	⎎
-	x	+	↑	⎍	⎎
x	-	+	+	-	+
x	-	↑	+	⎍	⎎
x	-	+	↑	⎍	⎎
+	↓	+	+	⎍	⎎
↓	↓	+	+	⎍	⎎
↓	+	+	+	⎍	⎎

SN 74123

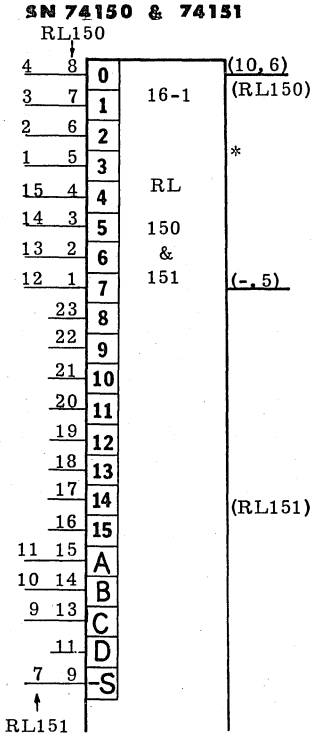


Single Shot

Inputs T_1, T_2, and T_3 are used for external RC networks to increase the time of the single shot. When a minus is present on the -R input it causes output Pin 4 to go minus and output Pin 13 to go positive.

+5 on Pin 16
GND on Pin 8

SN 74150 & 74151



16-Bit Data Selector

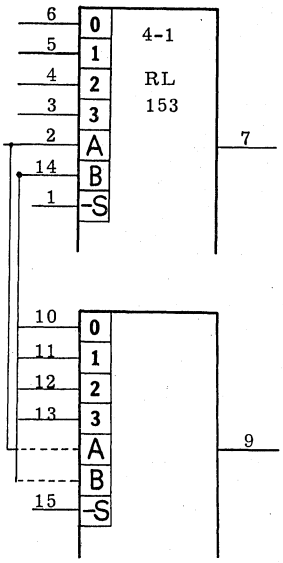
If -S is minus, Output Pin 10 will follow the selected input Pin, but will be inverted.

Pin	Selected Input Pin	
A B C	- Pin D	+
- - -	8	23
+ - -	7	22
- + -	6	21
+ + -	5	20
- - +	4	19
+ - +	3	18
- + +	2	17
+ + +	1	16

8-Bit Data Selector

RL151 is the same as RL150 except that there are only eight data inputs and no gating on Pin D. Use the same truth table but ignore the Pin D portion, for output pins 16 through 23.

SN 74153



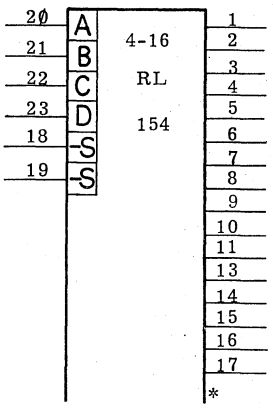
4 to 1 Data Selector

If either the Pin 1 or the Pin 15 input is minus, the output at Pin 7, or Pin 9, will be the same as the selected input.

Pin		Selected	
14	2	Input	Pin
-	-	6	10
+	-	5	11
-	+	4	12
+	+	3	13

+5 on Pin 16
GND on Pin 8

SN 74154



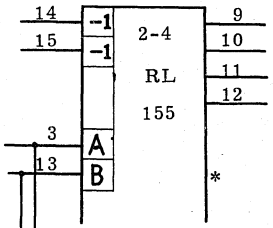
4-16 Decoder

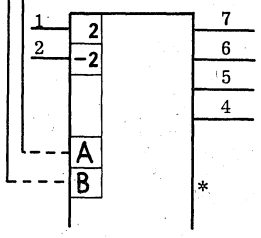
Pins 18 and 19 must be minus to change the output.

Pin				- on Pin
20	21	22	23	
-	-	-	-	1
-	-	-	+	2
-	-	+	-	3
-	-	+	+	4
-	+	-	-	5
-	+	-	+	6
-	+	+	-	7
-	+	+	+	8
+	-	-	-	9
+	-	-	+	10
+	-	+	-	11
+	-	+	+	13
+	+	-	-	14
+	+	-	+	15
+	+	+	-	16
+	+	+	+	17

+5 on Pin 24
GND on Pin 12

SN 74155





Dual 2-4 Decoder

Pins 14 and 15 must be minus to decode Pins 3 and 13.

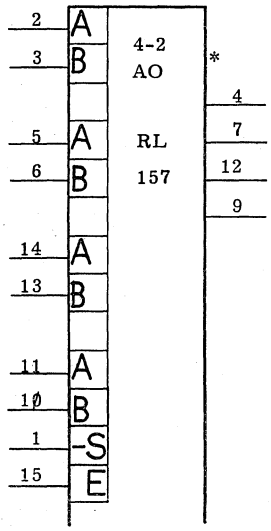
Pin		- on Pin
13	3	
-	-	9
+	-	10
-	+	11
+	+	12

Pin 1 must be plus, and Pin 2 must be minus to decode Pins 3 and 13.

Pin		- on Pin
13	3	
-	-	7
+	-	6
-	+	5
+	+	4

+5 on Pin 16
GND on Pin 8

SN 74157

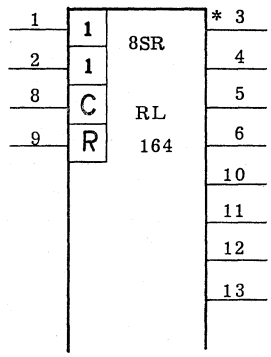


Quad 2-1 Selector

Output Pins 4, 7, 12 and 9 will follow the input Pins when Pin 15 is minus. If Pin 15 is plus, all outputs are minus.

INPUTS				Output Pins
15	1	A	B	
+	x	x	x	-
-	-	-	x	-
-	-	+	x	+
-	+	x	-	-
-	+	x	+	+
+5 on Pin 16 GND on Pin 8				

SN 74164

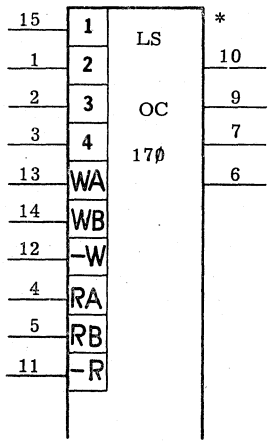


8-Bit Shift Register

The two 1 inputs are 'AND'ed at clock (C input) time. If both inputs are positive, Output Pin 3 will be positive. Every clock pulse causes Pin 3 to be set or reset; depending upon the 1 inputs, Pin 3 gated to Pin 4, Pin 4 to 5, Pin 5 to 6, etc. A positive pulse on input Pin 9 causes all outputs to go negative, effectively resetting the circuit.

+5 on Pin 14
GND on Pin 7

SN 74170



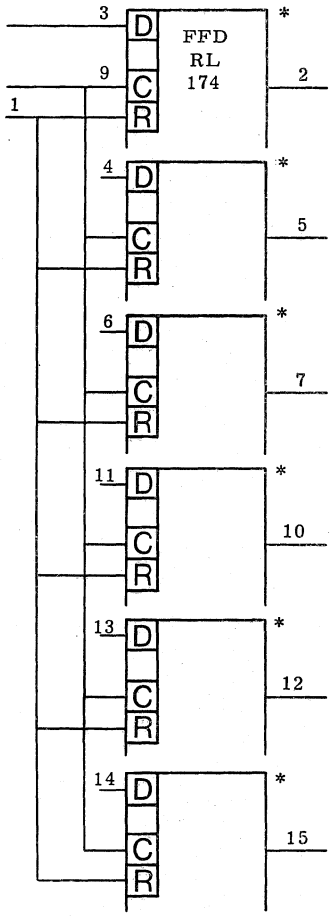
4 x 4 Local Store

Data input is on Pins 15, 1, 2 and 3. There are four registers per data input. The -W input gates the WA and WB inputs on Pins 13 and 14, which determine which one of the four registers will receive the data.

The -R input gates the RA and RB inputs on Pins 5 and 11. The RA and RB inputs determine which of the four sets of registers will be gated to output Pins 10, 9, 7 and 6. Pin 1Ø output contains data from input Pin 15; Pin 9 reflects data from Pin 1; Pin 7 from Pin 2; and Pin 6 from Pin 4.

+5 on Pin 16
GND on Pin 8

SN 74174



Hex D-Type Flip-Flop

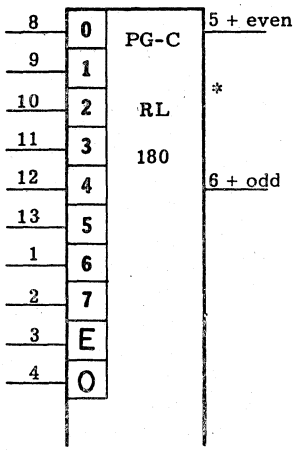
Level on pin 3 (D) at clock time (+ transition) is gated to pin 2 and maintained until the next clock pulse. All six FF's share the same clock pulse.

The common Clear (R) line resets all FF outputs to -.

Inputs			Outputs
R	C	D	Q
-	x	x	-
+	↑	+	+
+	↑	-	-
+	-	x	No change

x = irrelevant
↑ = transition from low to high level.

SN 74180 & SN 75180

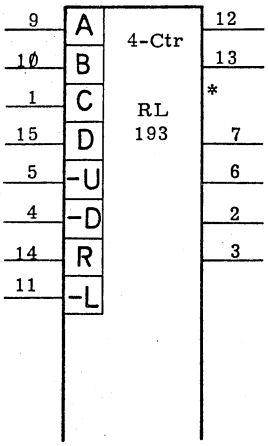


Parity Generator Checker

Output Pin 5 is the parity check output. Output Pin 6 is the parity bit output. Input Pins 3 and 4 determine parity checking for Odd or Even parity in accordance with the following truth table.

+ INPUTS	GATES		+ OUTPUT
BIT 0 - 7	E	O	
Even	+	-	Even
Odd	+	-	Odd
Even	-	+	Odd
Odd	-	+	Even
Either	+	+	Neither
Either	-	-	Both

SN 74193



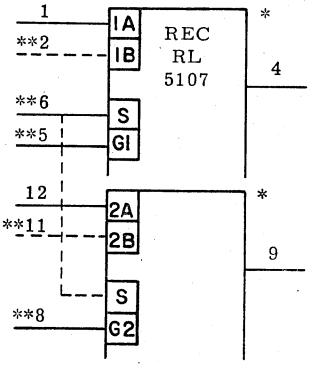
4-Bit Binary Up-Down Counter

Input Pins 9, 10, 1 and 15 are used to load the initial value into the counter, which then counts up once for every minus pulse on input Pin 5. The counter counts down for every minus pulse on input Pin 4. A plus on input Pin 14 resets the counter. A minus on input Pin 11 gates bits A, B, C and D into the counter. A minus on output Pin 12 indicates a carry, which a minus on Pin 13 indicates the counter counted through zero. Outputs 3, 2, 6 and 7 reflect the current value of the counter.

Binary	
Pin	Value
3	1
2	2
6	4
7	8

+5 on Pin 16
GND on Pin 8

SN 75107

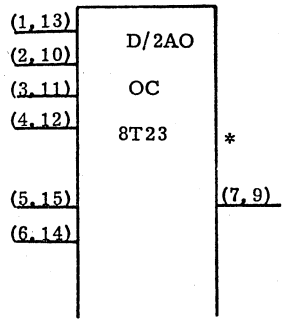


Special Purpose Line Receiver

Used with CII IRIS I/O interface only. For this application, pins 4, 5, 8, and 9 are tied to +5V. Inputs 1B and 2B are biased to +.65V to achieve a +1.6V "1's" detection threshold at inputs 1A and 2A. Nominal interface levels are ground and +2V.

+5 on pin 14
-5 on pin 13
Gnd on pin 7
** (For CII)
Pins 5, 6, and 8 tied to +5V.
Pins 2, and 11 tied to +.65V.

8T23



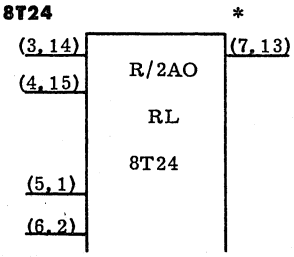
Dual Line Driver

Special Line Driver compatible with IBM System/360 I/O Interface Specifications.

The output (Pin 7) is plus when input Pins 1, 2, 3 and 4 or Pins 5 and 6 are plus.

+5 on Pin 16
GND on Pin 8

8T24

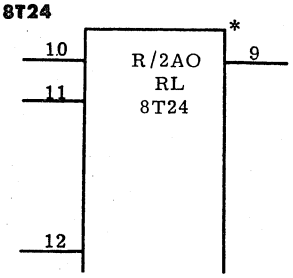


Triple Line Receiver

Special Line Receiver compatible with IBM System/360 I/O Interface Specifications.

The output (Pin 7) is plus when input Pins 3 and 4, or 5 and 6 go plus.

8T24



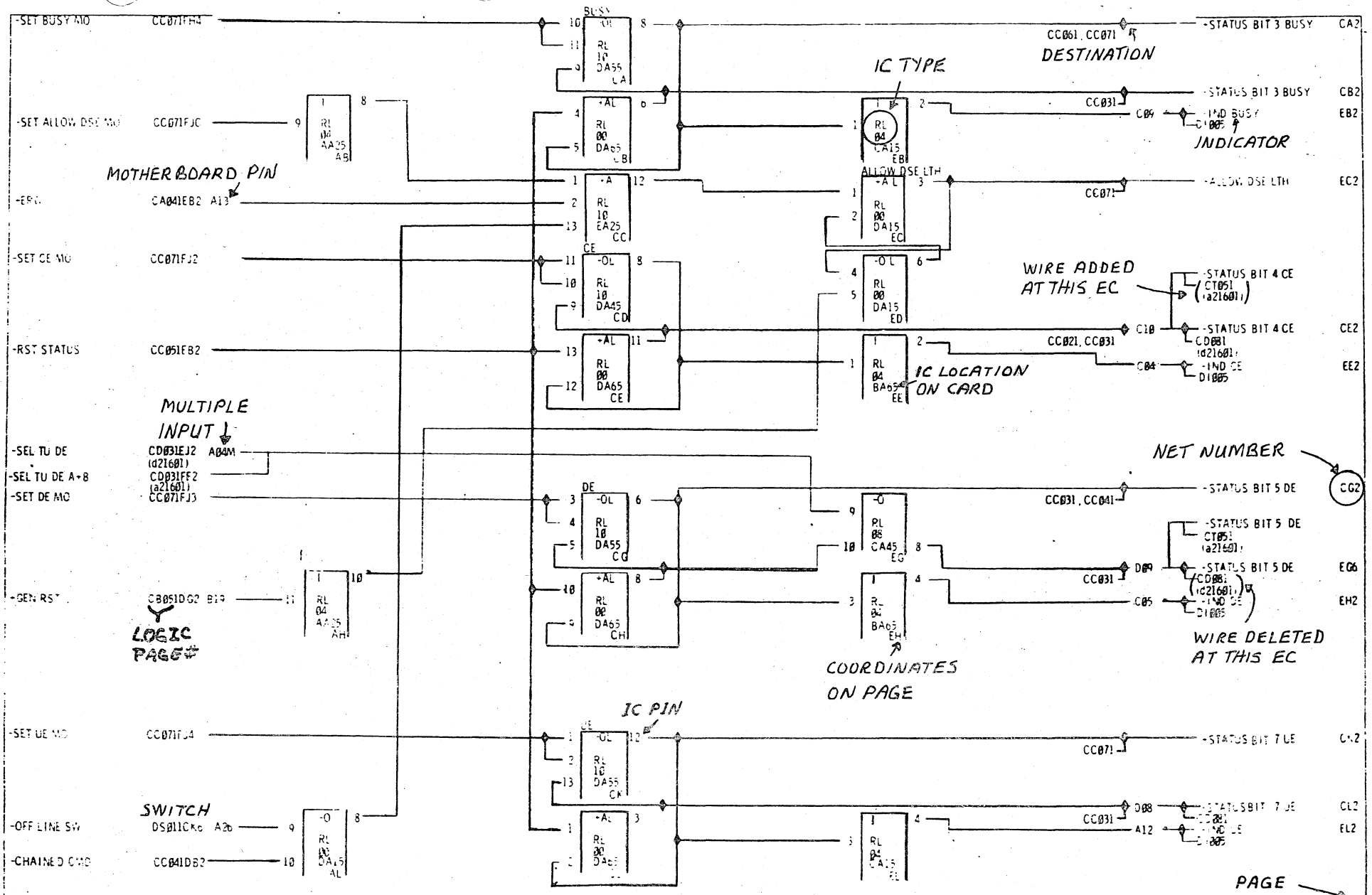
Output Pin 9 is plus when input Pins 10 and 11, or Pin 12 goes plus.

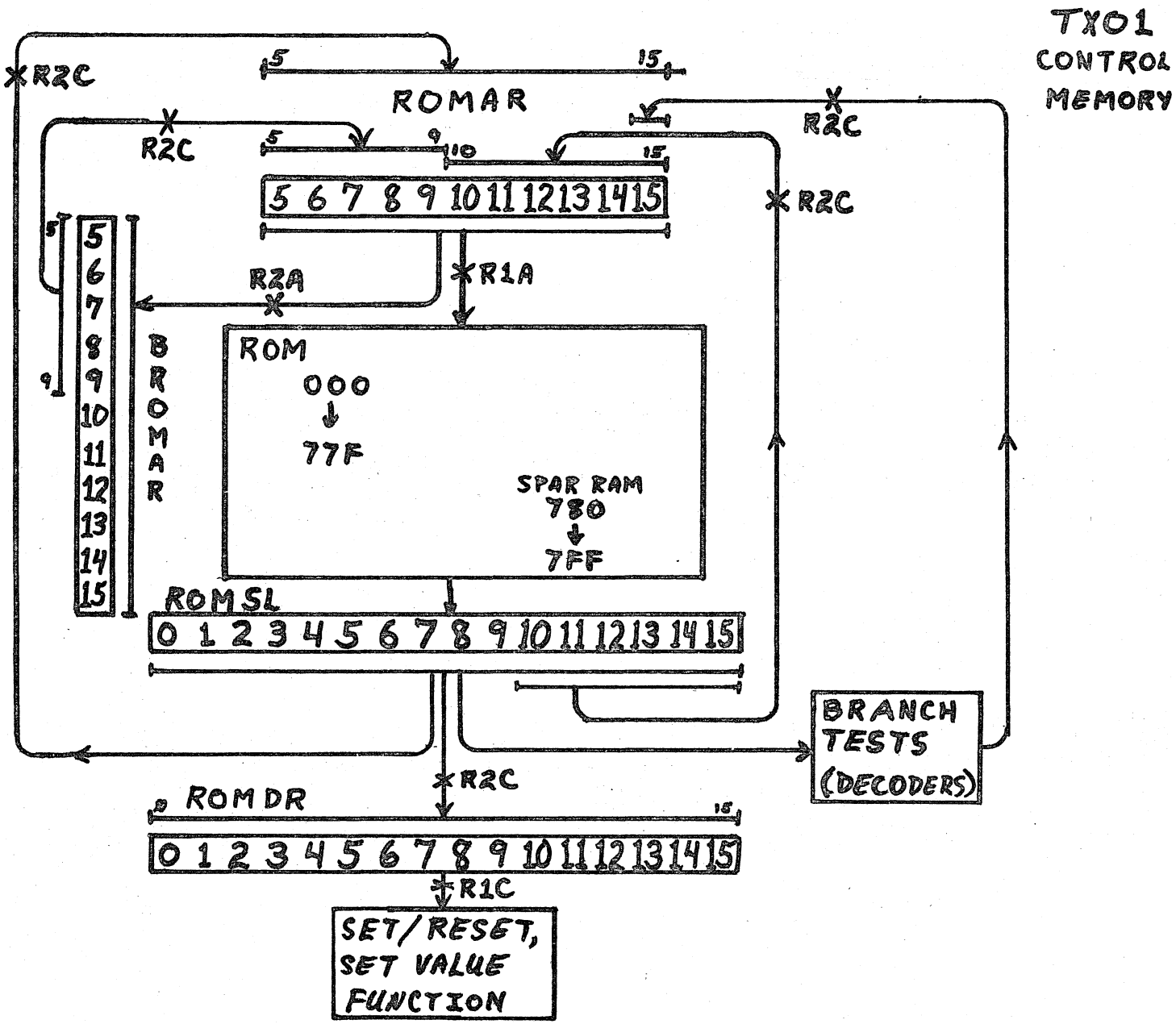
+5 on Pin 16
GND on Pin 8

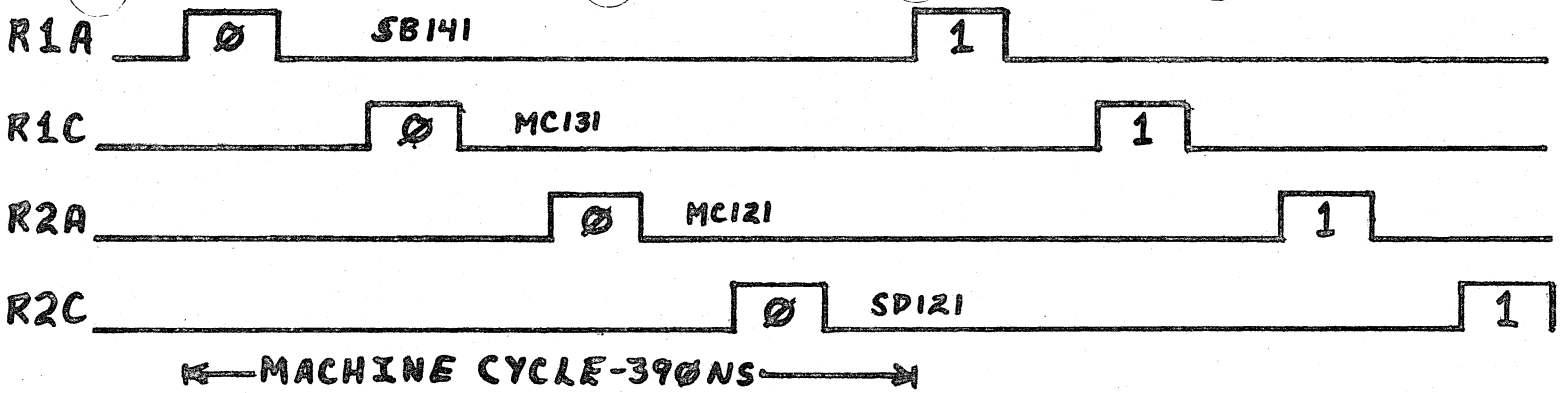
Notes:

1. The first output or input pin number applies to the first circuit of a series of two or more identical circuits of the same IC.
2. Ground is normally connected to Pin 7 and VDC input to Pin 14 unless otherwise specified.
3. Supply voltage (VDC) is between 4.75 and 5.25 with respect to ground (GND) unless otherwise specified (7 VDC max).
4. The asterisk (*), which is located on the output side of some blocks, indicates inverted outputs are above the asterisk and the non-inverted outputs are below.
5. Output signals of STC equipment are normally grounded or at +4.0 volts DC.

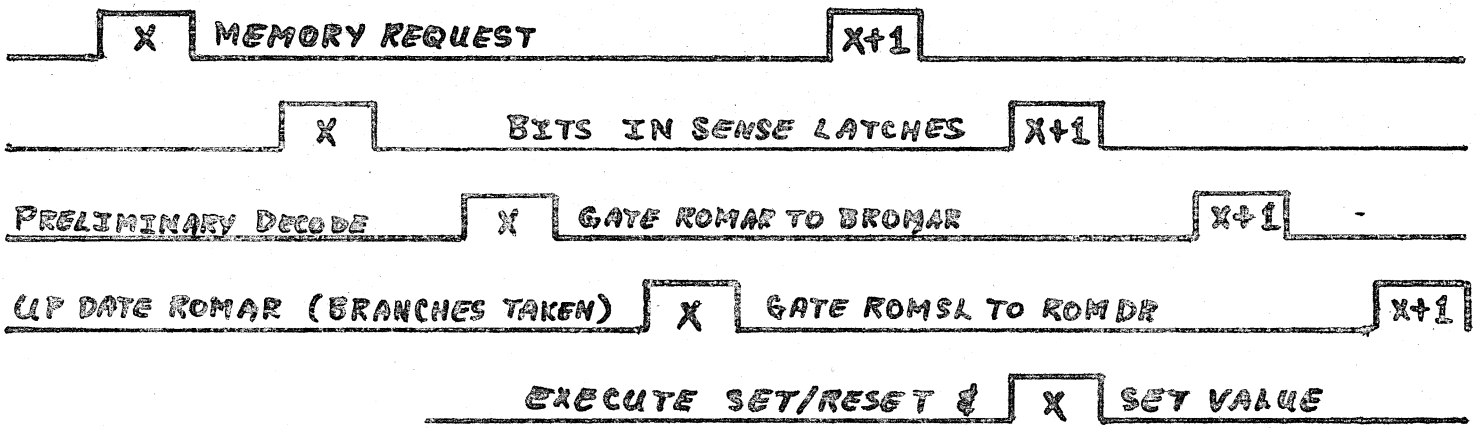
8

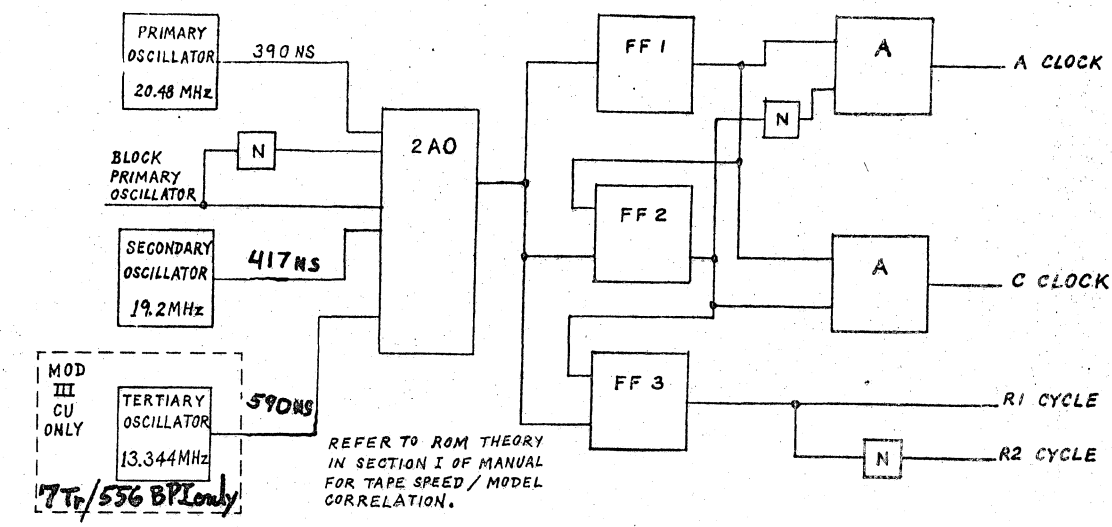

-SET BUSY M0
CC071FH4
BUSY
-STATUS BIT 3 BUSY
CA2
CC061, CC071
DESTINATION
IC TYPE
-SET ALLOW DSE M0
CC071FJC
-STATUS BIT 3 BUSY
CB2
CC031
-IND BUSY
EB2
INDICATOR
MOTHERBOARD PIN
-ALLOW DSE LTH
EC2
CC071
-EPC
CA041EB2 A13
-SET CE M0
CC071FJ2
CE
WIRE ADDED AT THIS EC
-STATUS BIT 4 CE
CT051 (a21601)
-STATUS BIT 4 CE
CE2
CC021, CC031
-IND CE
EE2
-RST STATUS
CC051EB2
IC LOCATION ON CARD
MULTIPLE INPUT
-SEL TU DE
CD031EJ2 (d21601) A04M
-SEL TU DE A+B
CD031FF2 (a21601)
-SET DE M0
CC071FJ3
DE
NET NUMBER
CG2
-STATUS BIT 5 DE
CC031, CC041
-STATUS BIT 5 DE
CT051 (a21601)
-STATUS BIT 5 DE
EG6
CC031
-IND DE
EH2
-GEN RST
CB051DG2 B19
LOGIC PAGE#
WIRE DELETED AT THIS EC
COORDINATES ON PAGE
IC PIN
-SET UE M0
CC071FJ4
UE
-STATUS BIT 7 UE
CK2
CC071
-STATUS BIT 7 UE
CL2
CC031
-IND UE
EL2
SWITCH
-OFF LINE SW
DS011CK0 A26
-CHAINED CMD
CC041DB2
EXIT FROM MOTHER BOARD
MASTER MOD
PAGE
STATUS BIT 3 4 5 7
PRESENT E C 21600
DATE 9-12-70
CD LOC 01A-A3C2
PREV E C 21093
PG PN 30755
CD TYPE CC
MACH 3800-1


TX01
CONTROL
MEMORY
R2C
5
15
ROMAR
R2C
5
9
10
15
R2C
5 6 7 8 9 10 11 12 13 14 15
R2C
5
6
7
8
9
10
11
12
13
14
15
9
BROMAR
R2A
R1A
ROM
000
77F
SPAR RAM
780
7FF
ROMSL
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
BRANCH
TESTS
(DECODERS)
R2C
ROMDR
0
15
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
R1C
SET/RESET,
SET VALUE
FUNCTION



R1A. MEMORY REQUEST TO ROM
R1C. BITS ARE IN SENSE LATCHES
R2A. PRELIMINARY DECODE, GATE ROMAR TO BROMAR
R2C. UP DATE ROMAR (BRANCHES TAKEN), GATE ROMSL TO ROM DR (IF SET/RESET)
R1A, (NEXT) MEMORY REQUEST TO ROM
R1C, EXECUTE SET/RESET & SET VALUE INSTRUCTIONS





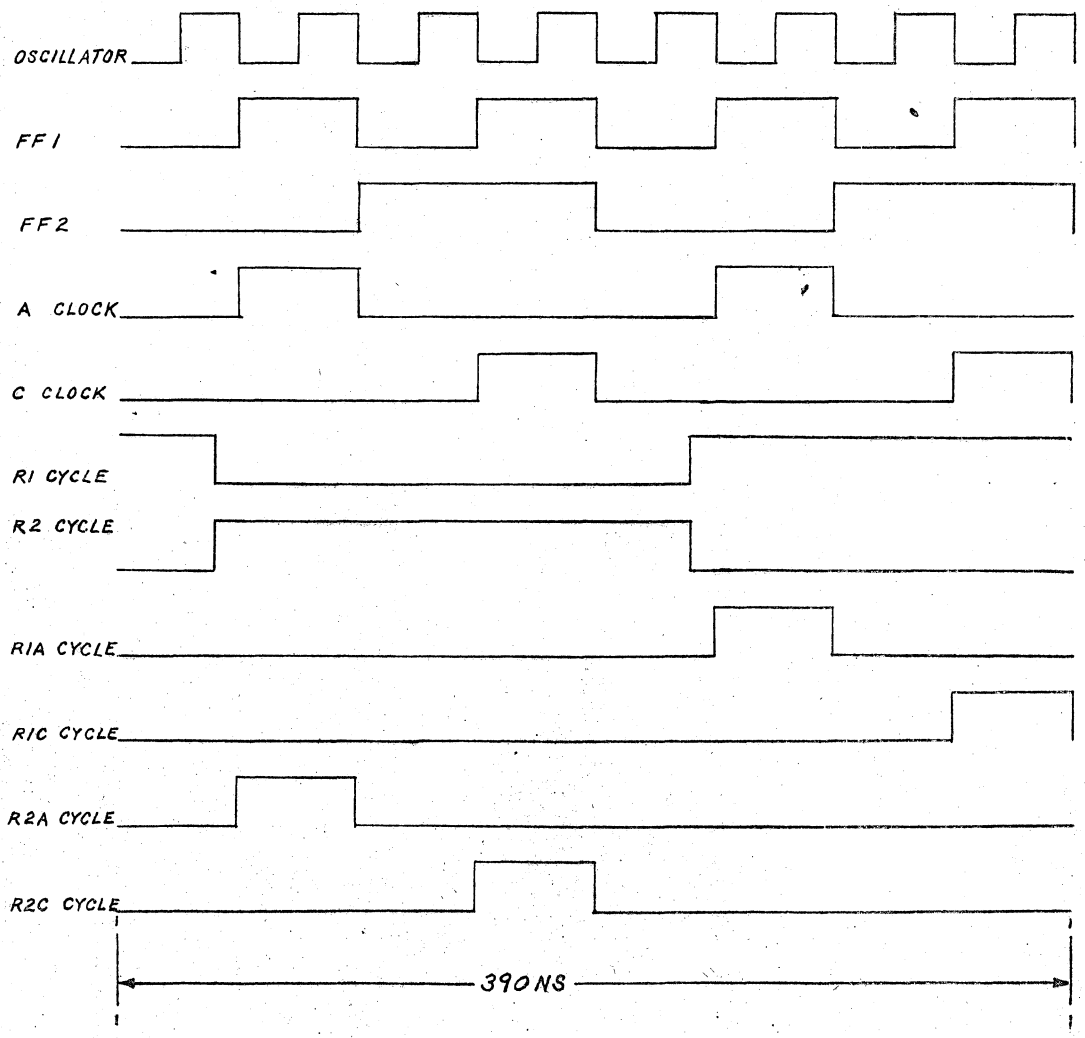
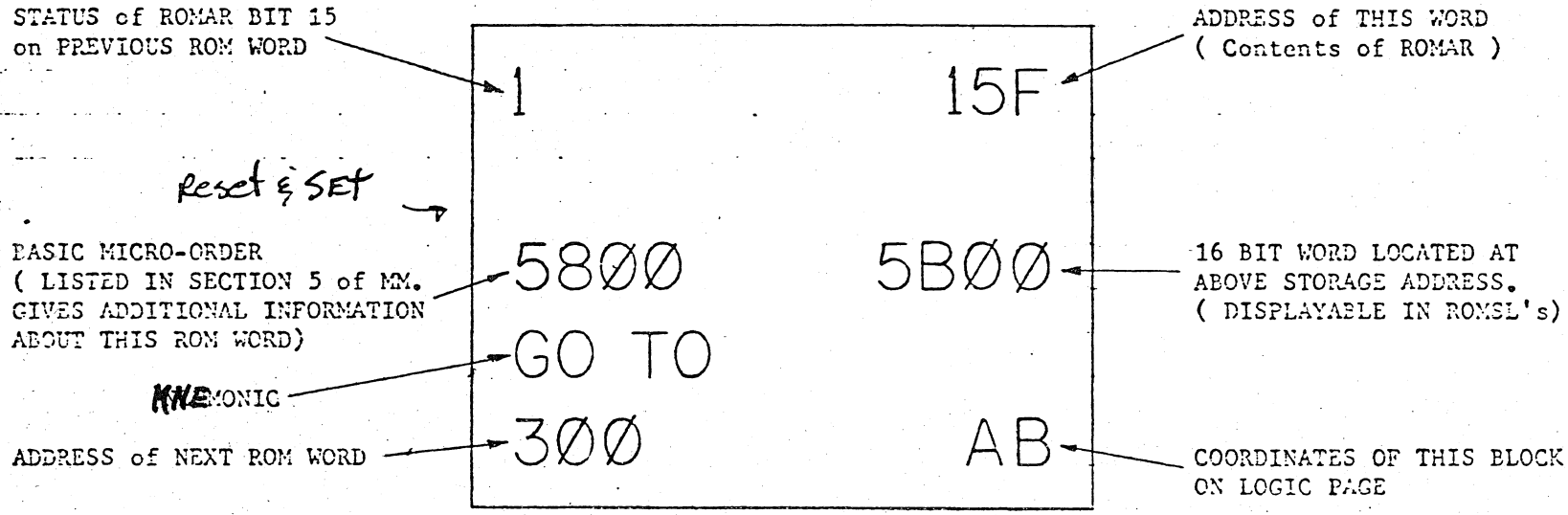
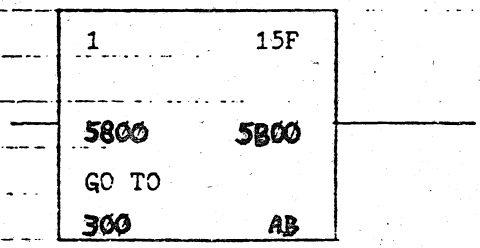
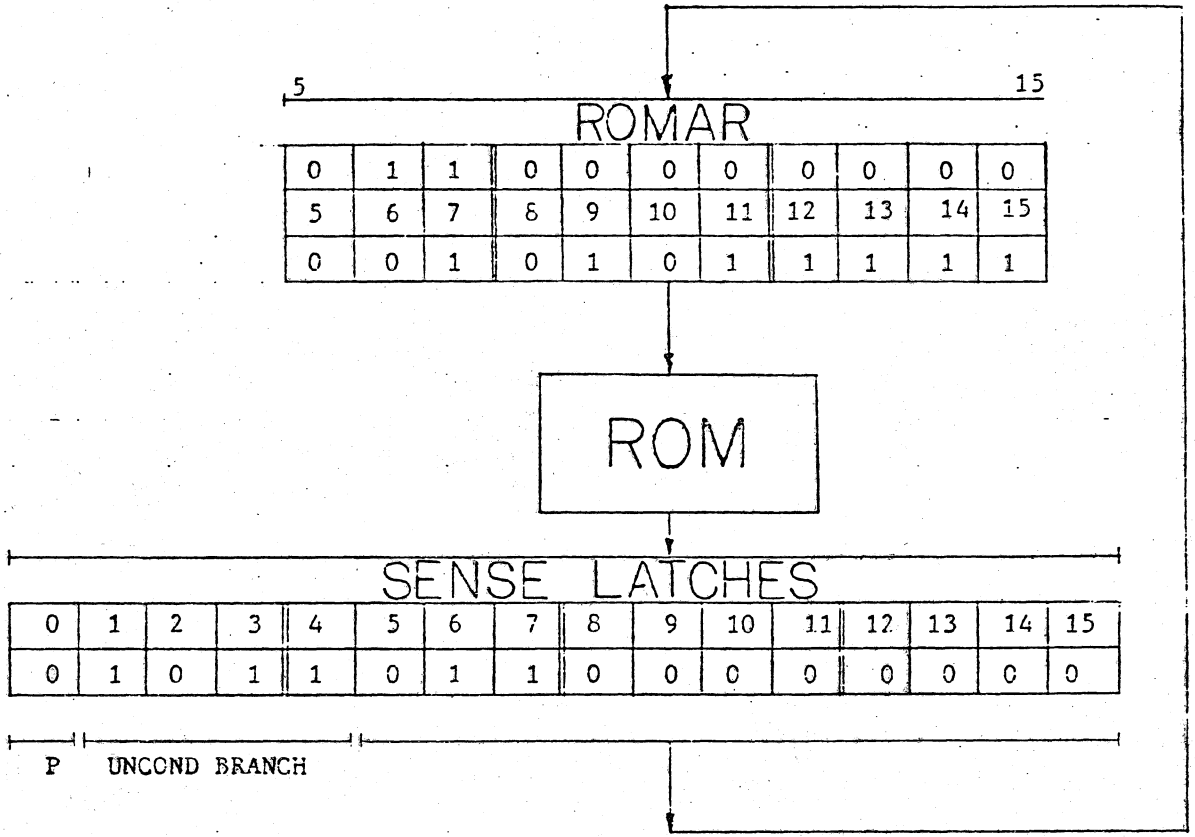


Figure 3-8. Control Unit Clocks.



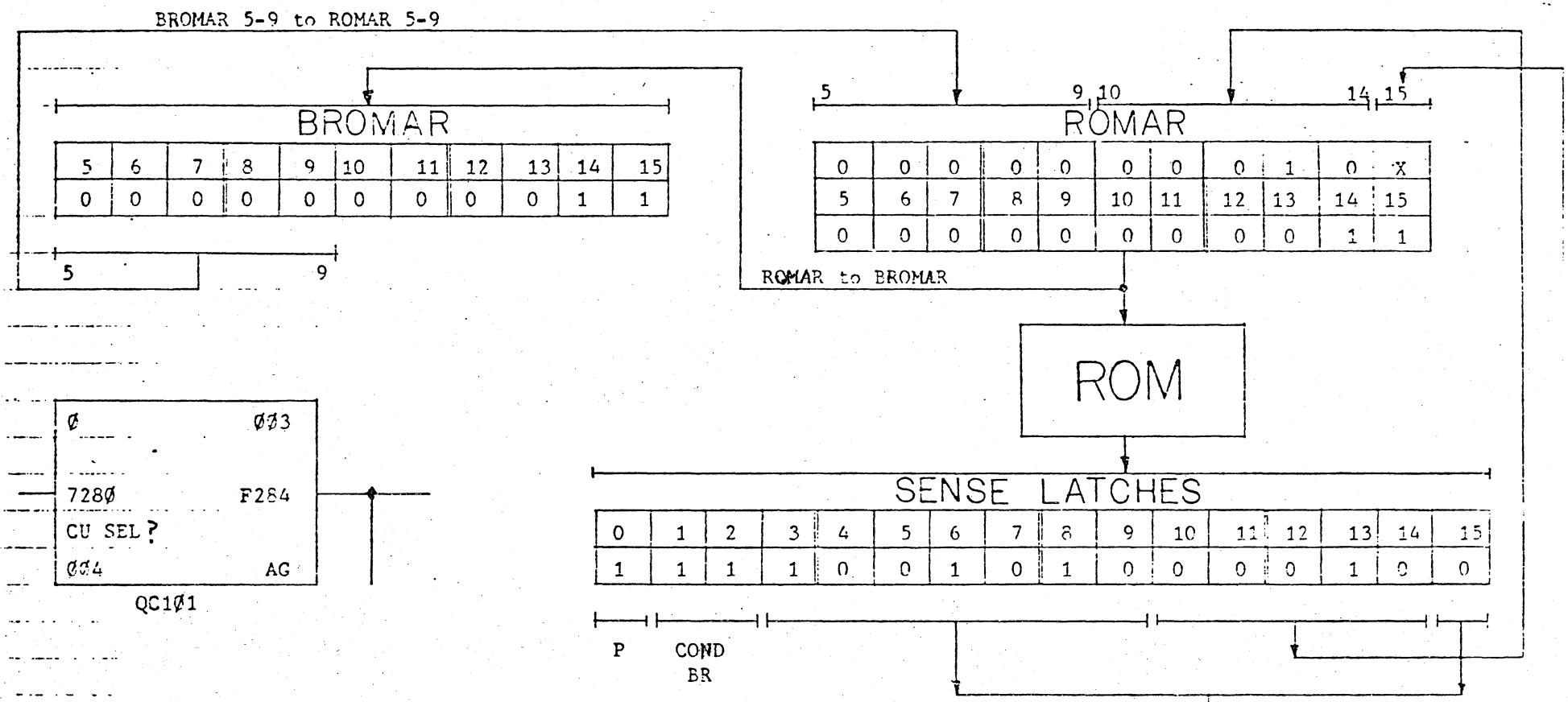
THE ROM LOC BLOCK





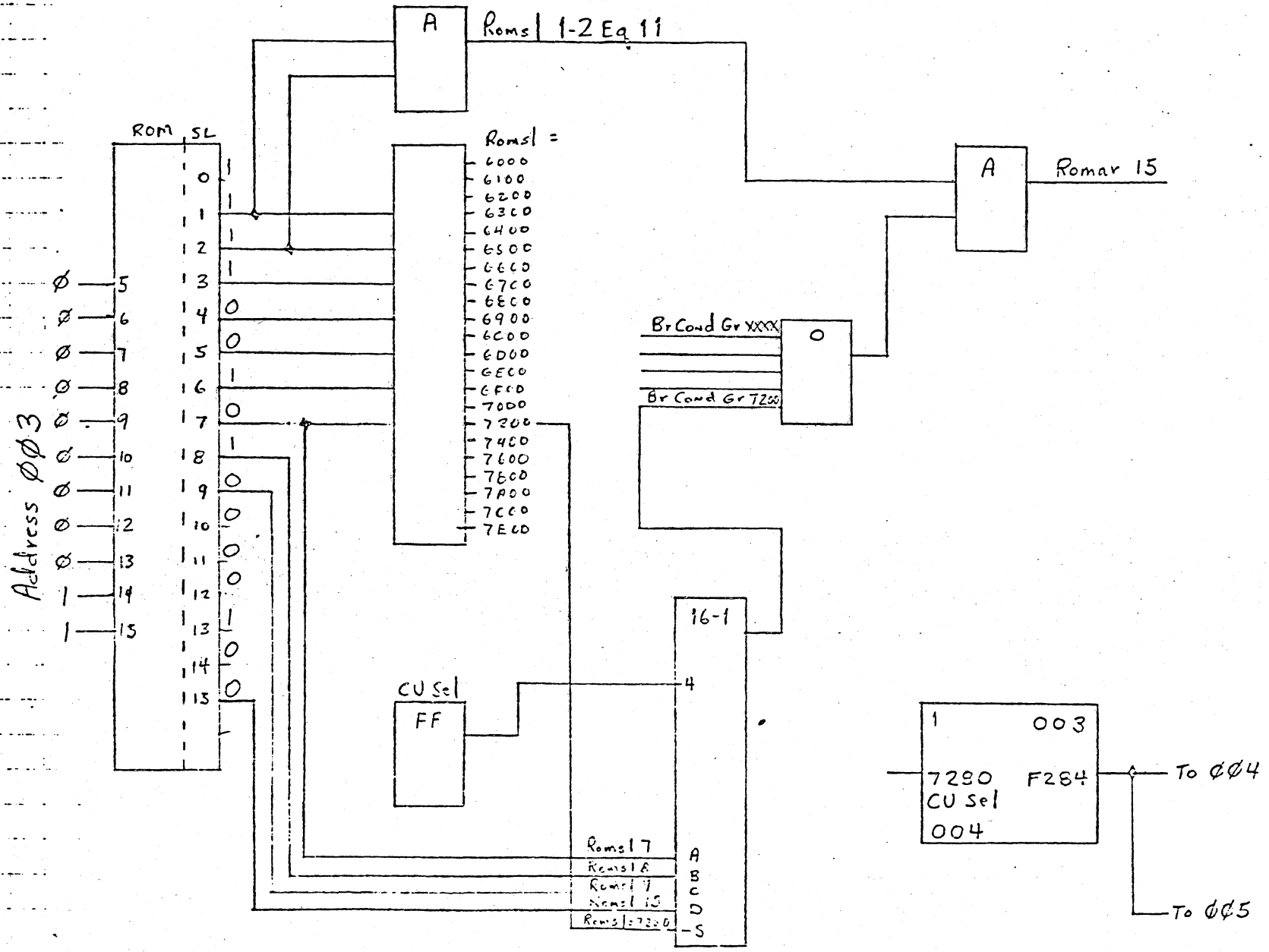
1. Decode: Bits 1,3, and 4 on; bit 2 off.
2. Bits 5-15 of the ROMSL's will be gated to ROMAR to become the next address.

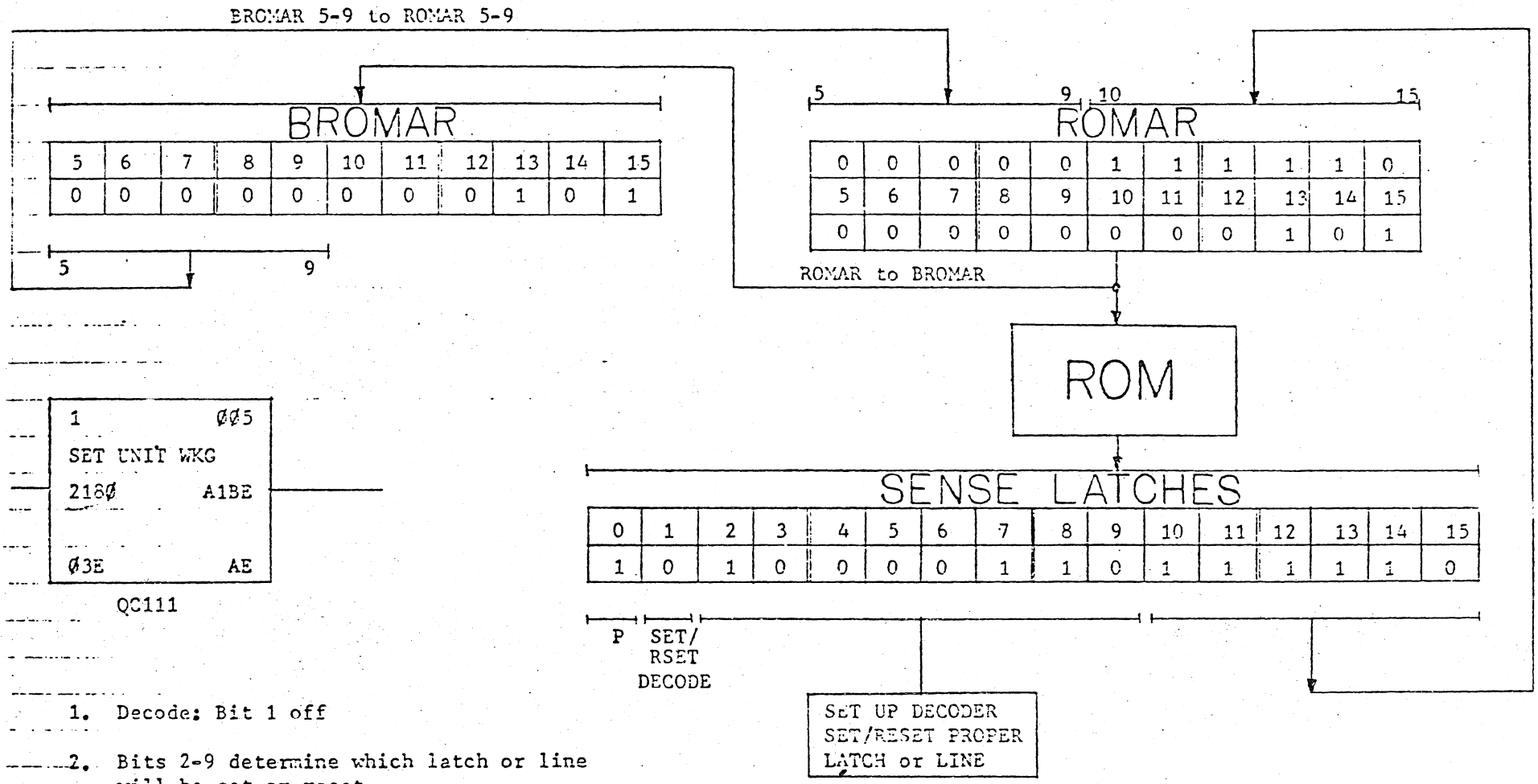
Unconditional Branch



1. Decode: Bits 1&2 on
2. Bits 3-9 and 15 set up branch condition
3. To form next address:
   a. BROMAR 5-9 to ROMAR 5-9
   b. ROMSL 10-14 to ROMAR 10-14
   c. ROMAR 15 is result of branch decision

CONDITIONAL BRANCH


A
Roms| 1-2 Eq 11
ROM SL
Address ØØ3
Roms| =
6000
6100
6200
6300
6400
6500
6600
6700
6800
6900
6A00
6B00
6C00
6D00
6E00
6F00
7000
7200
7400
7600
7800
7A00
7C00
7E00
A
Romar 15
Br Cond Gr XXXX
Br Cond Gr 7200
0
16-1
CU Sel
FF
4
Roms|7
Roms|8
Roms|7
Roms|15
Roms|7200
A
B
C
D
S
1
003
7280
CU Sel
004
F284
To ØØ4
To ØØ5



1	ØØ5
SET UNIT WKG	
218Ø	A1BE
Ø3E	AE

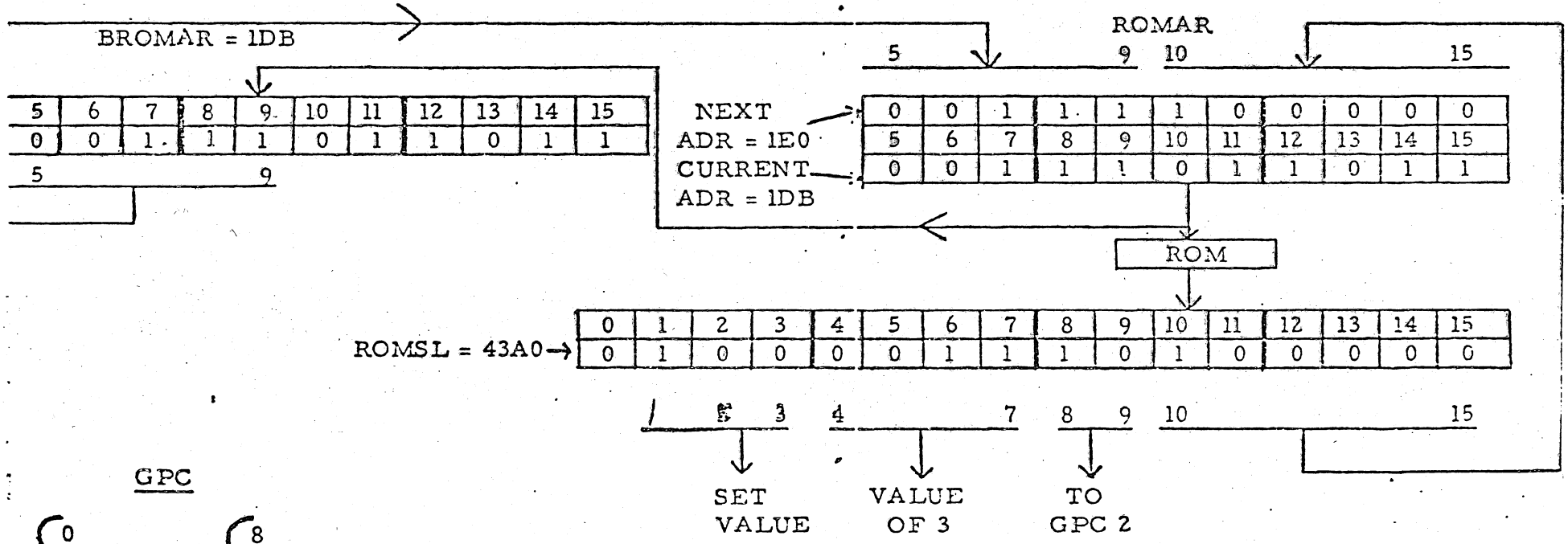
QC111

1. Decode: Bit 1 off
2. Bits 2-9 determine which latch or line will be set or reset.
3. To form next address:
   a. BROMAR 5-9 to ROMAR 5-9
   b. ROMSL 10-15 to ROMAR 10-15

SET/RESET

SET VALUE:

- BITS 2 & 3 OFF, 1 ON.
- THE BINARY VALUE OF SENSE LATCHES 4 - 7 WILL BE TRANSFERRED TO THE GPC REGISTER DESIGNATED BY THE BINARY VALUE OF BITS 8 & 9.
- NEXT ROMAR ADDRESS IS CONSTRUCTED BY TAKING BITS 5 - 9 FROM BROMAR AND BITS 10 - 15 FROM SENSE LT'S 10 - 15.



5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	1	0	1	1	0	1	1

	0	0	1	1	1	1	0	0	0	0	0
NEXT ADR = 1E0	5	6	7	8	9	10	11	12	13	14	15
CURRENT ADR = 1DB	0	0	1	1	1	0	1	1	0	1	1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	0	0	0	1	1	1	0	1	0	0	0	0	0

GPC

0		8
1	2	9
2		10 X
3		11 X
4		12
5	3	13
6		14
7		15

1	1DB
SET GPC 2-3	
4 3 8 Ø	4 3 A Ø
1 E 0	B H

WRITE OPERATION

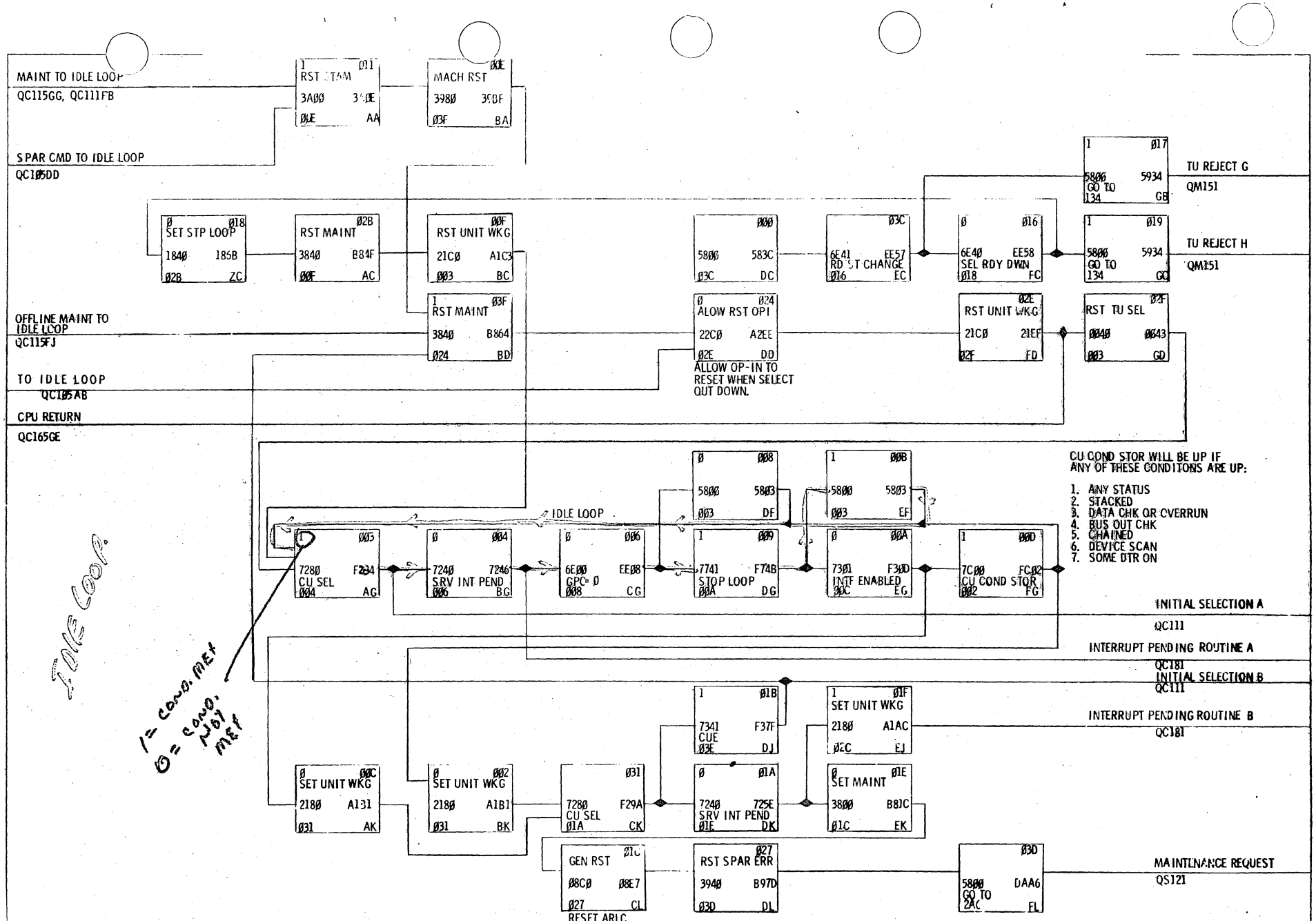
Following, are the pages and exits one should go through while executing a write command (01) on a TU70 at load point.

Page	Function	Exit
2-3	Initial Selection	B
2-4	Check Bus out parity and Command Decode	E
2-5	Present Initial Status	I
2-6	Resets after Status	Exec. Cmmds.
2-11	Write Prefetch	Motion Ctrl.
2-13	Motion Control (check bkwd status of drive)	C
2-16	Turnaround Delay	Q
2-15	Turnaround Delay---Set Write Status	N
2-13	Set BCR Value	A
2-14	Turnaround Complete	H
2-21	Load Point Delay	Write Seq.
2-27	Check Sta B trigger (LP)	B
2-31	Write PE ID Burst	J
2-32	Create Gap between ID Burst and Record	K
2-27	Write Leading 40 Zeros	D
2-28	Write Data Loop	E
2-29	Read Back Check	H
2-30	Look for IBG, then Reset Go---Set Channel End	X
2-20	Resets, Set DE	End Seq. K
2-5	Present Final Status	J
2-6	Resets	To Online Wait Loop

TX01 READ OPERATION

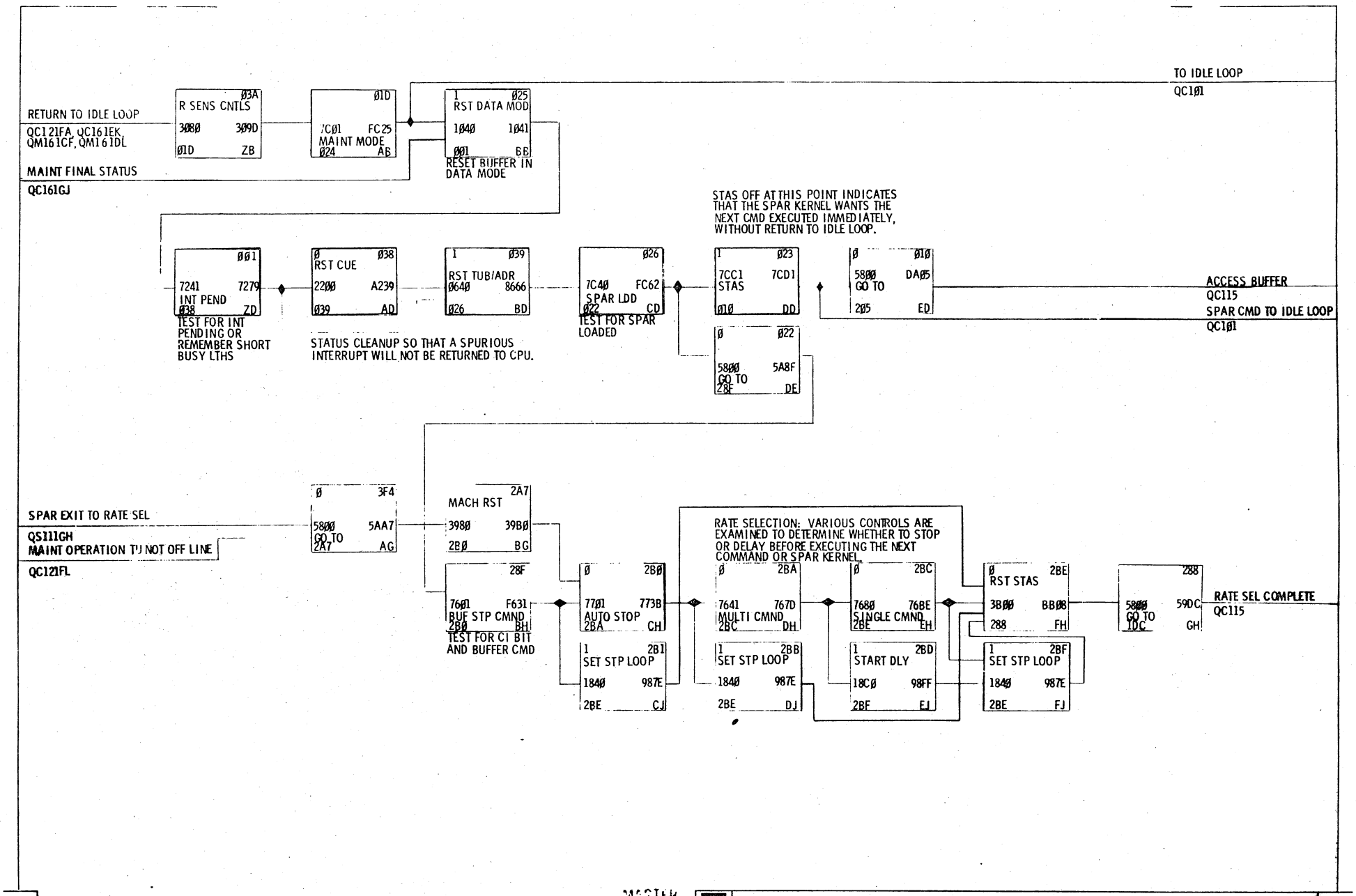
Following, are the pages and exits one should go through while executing a Read command on 9 track TU70.

2-3	Initial Selection	B
2-4	Check Bus Out Parity and Command Decode	F
2-7	Command Decode	DD
2-5	Present Initial Status	I
2-6	Resets/after STatus	EXECUTE Commands
2-11	Write Prefetch	Motion Ctrl.
2-13	Motion Control	A
2-14	Turnaround Complete	E
2-20	Generate Resets	Z
2-18	Turnaround Complete	V
2-19	Read Data Control	X
2-20	Generate Resets	Go to END Seq. K
2-5	Present Initial Status	J
2-6	Resets/After Status	Wait Loop

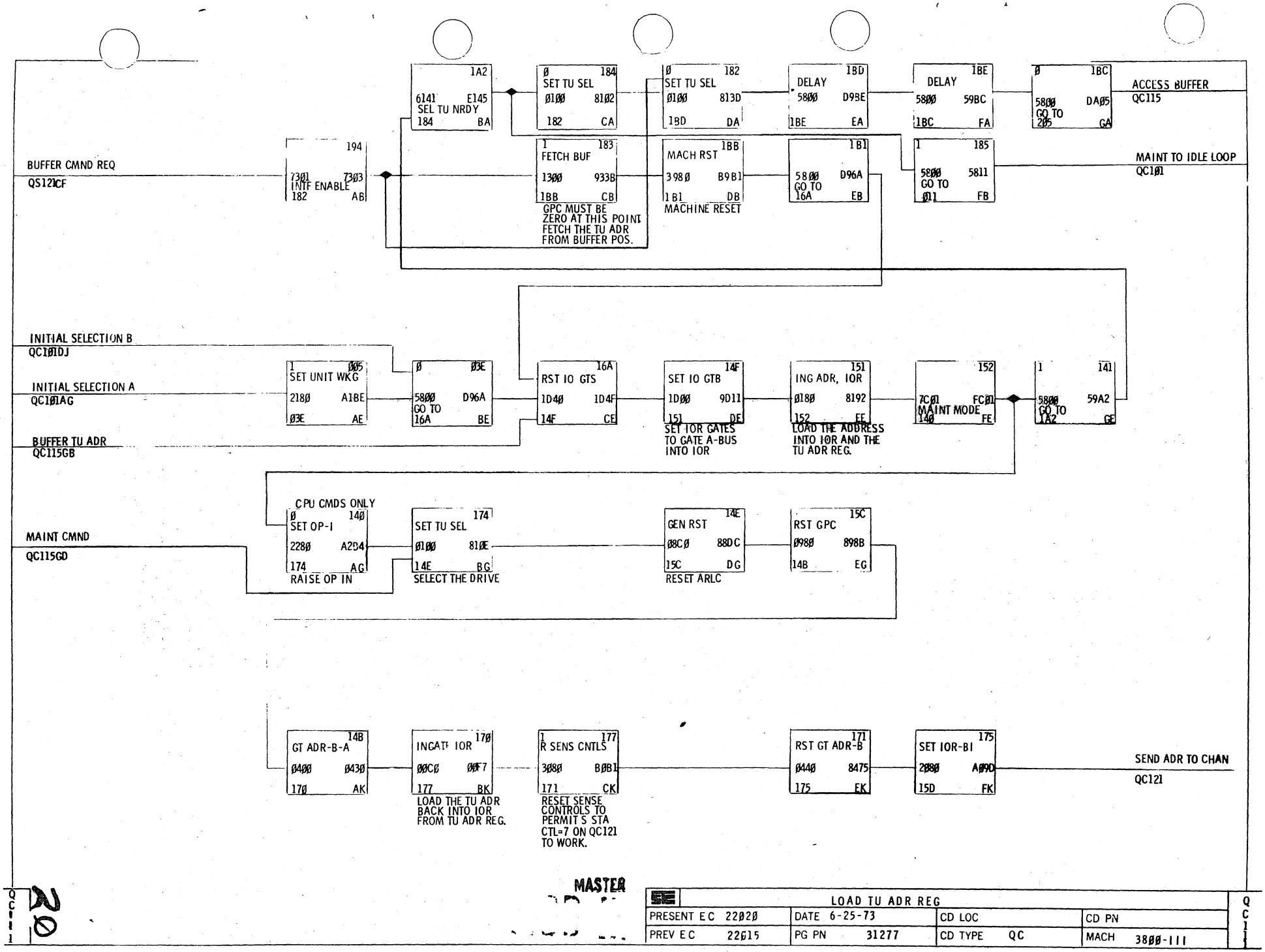


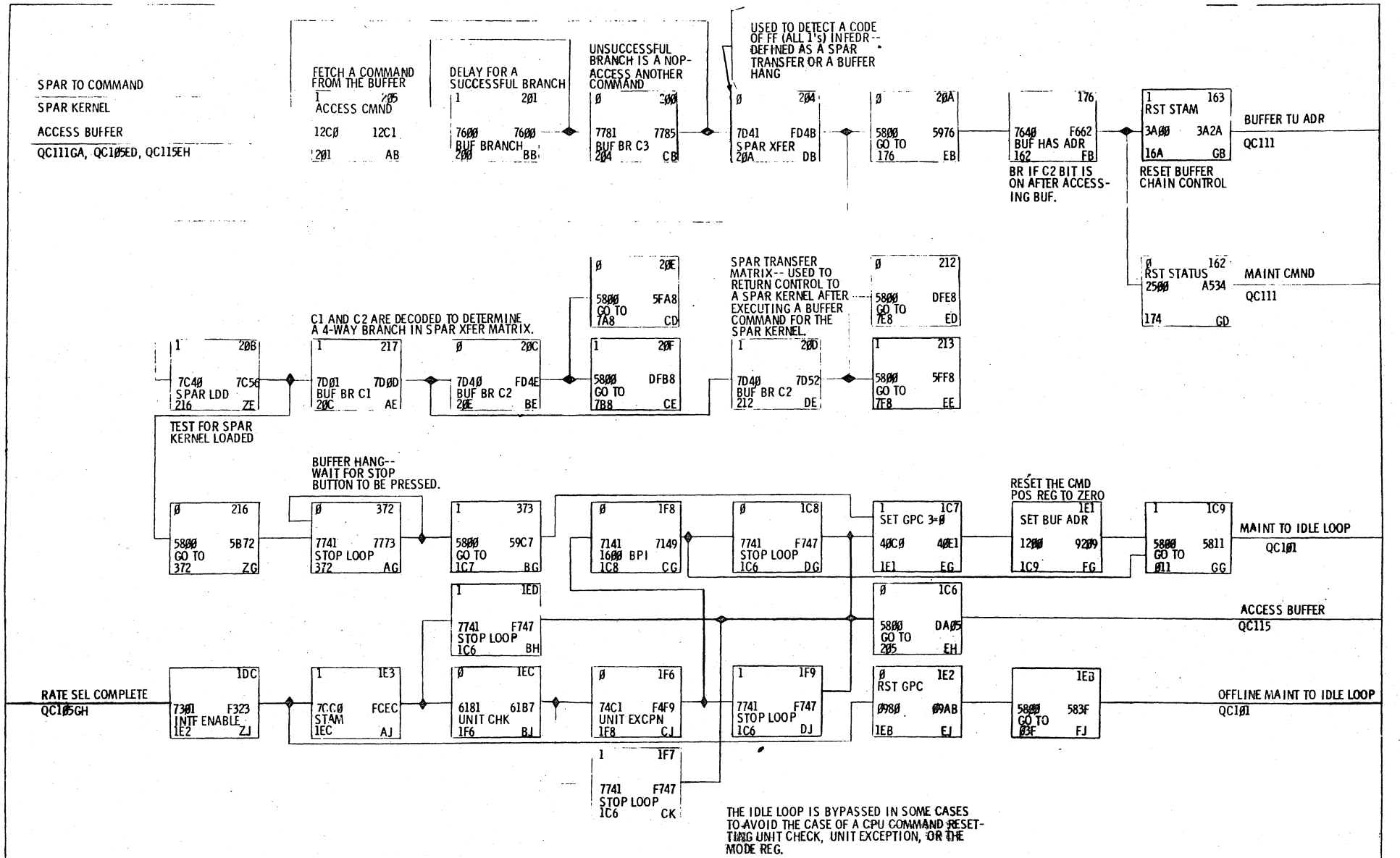
IDLE LOOP			
PRESENT EC 22020	DATE 7-9-73	CD LOC	CD PN
PREV EC 22015	PG PN 31275	CD TYPE QC	MACH 3800-111

QC101 19 QC101

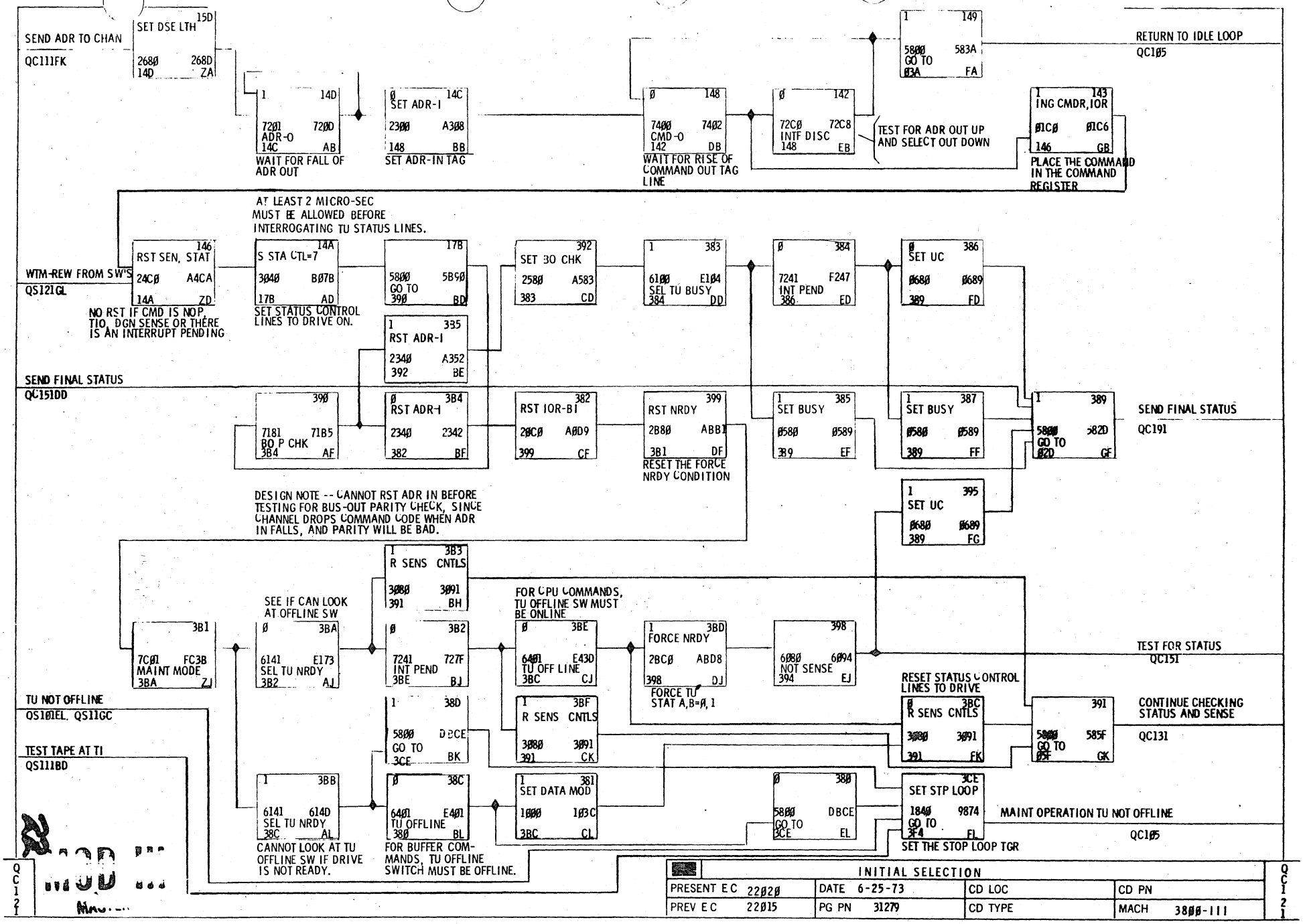


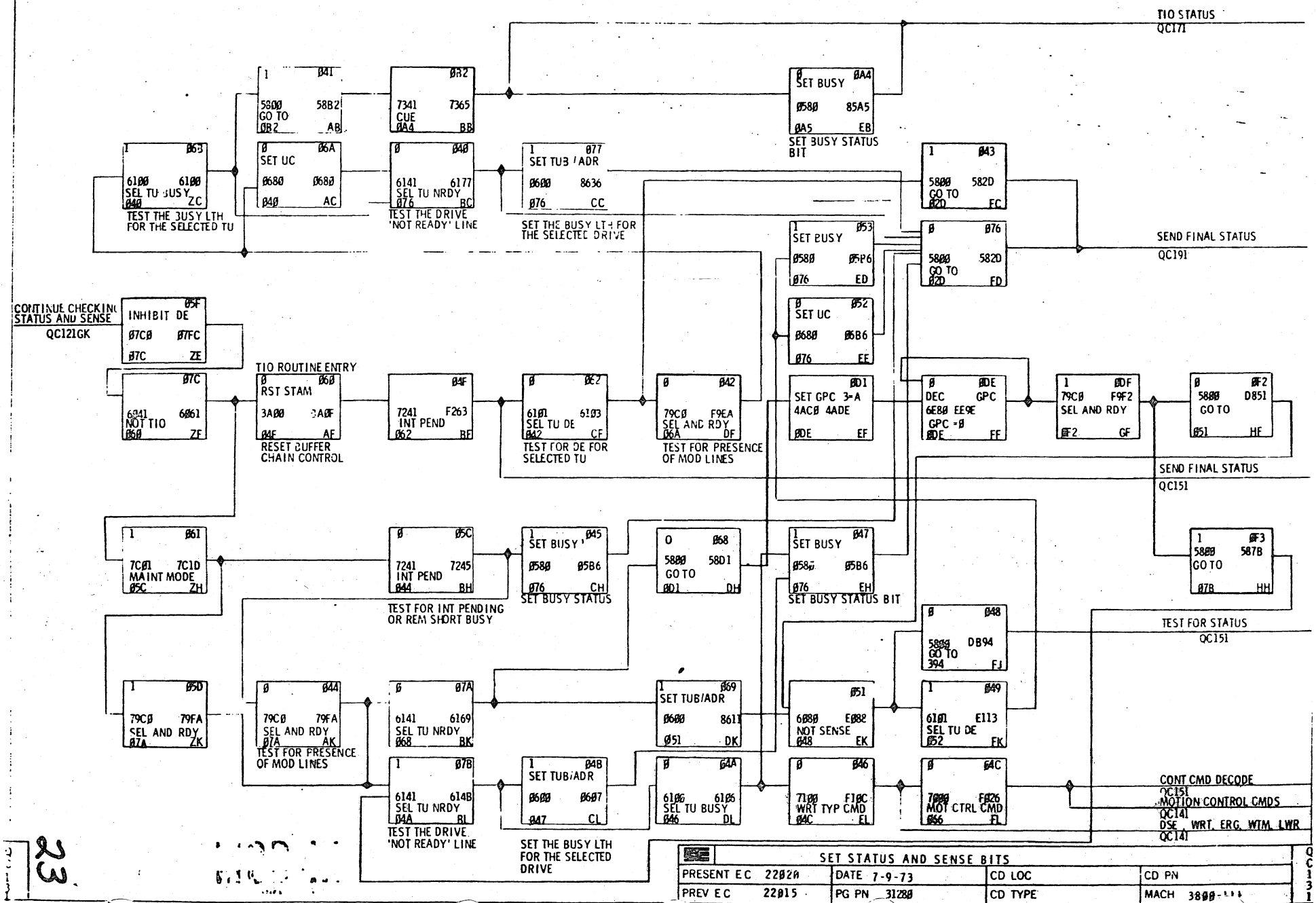
MAINT DELAY AND RATE SEL				
PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22015	PG PN 31276	CD TYPE QC	MACH 3800-111	

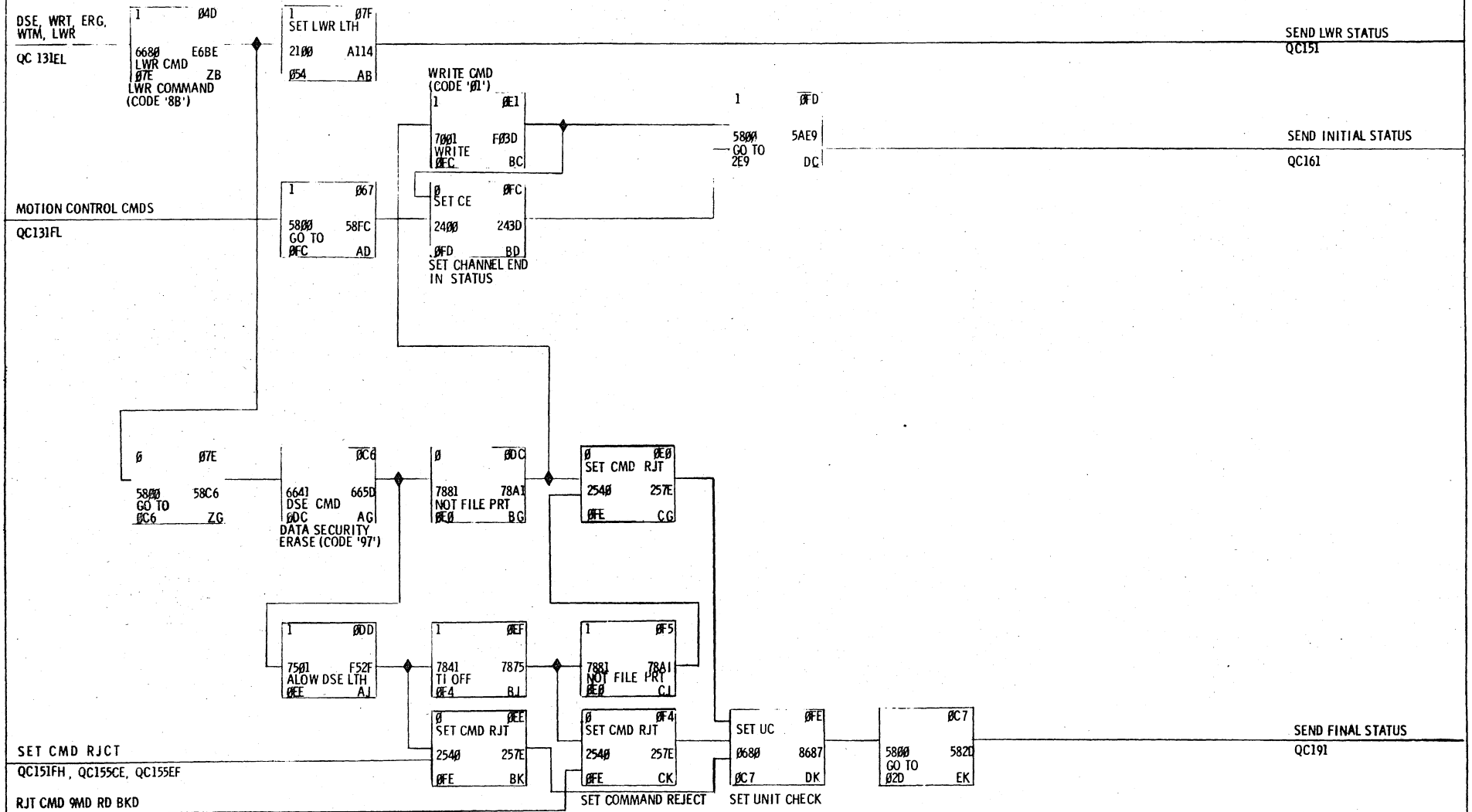

1A2
6141 E145
SEL TU NRDY
184 BA
Ø 184
SET TU SEL
Ø1ØØ 81Ø2
182 CA
Ø 182
SET TU SEL
Ø1ØØ 813D
1BD DA
1BD
DELAY
58ØØ D95E
1BE EA
1BE
DELAY
58ØØ 59BC
1BC FA
Ø 1BC
58ØØ DAØ5
GO TO
2Ø5 GA
ACCESS BUFFER
QC115
BUFFER CMND REQ
QS121CF
194
7301 7303
INTF ENABLE
182 AB
1 183
FETCH BUF
13ØØ 933B
1BB CB
GPC MUST BE
ZERO AT THIS POINT
FETCH THE TU ADR
FROM BUFFER POS.
1BB
MACH RST
398Ø B9B1
1B1 DB
MACHINE RESET
1B1
58ØØ D96A
GO TO
16A EB
1 185
58ØØ 5811
GO TO
Ø11 FB
MAINT TO IDLE LOOP
QC1Ø1
INITIAL SELECTION B
QC1Ø1DJ
INITIAL SELECTION A
QC1Ø1AG
BUFFER TU ADR
QC115GB
1 ØØ5
SET UNIT WKG
218Ø A1BE
Ø3E AE
Ø 03E
58ØØ D96A
GO TO
16A BE
16A
RST IO GTS
1D4Ø 1D4F
14F CE
14F
SET IO GTB
1DØØ 9D11
151 DE
SET IOR GATES
TO GATE A-BUS
INTO IOR
151
ING ADR, IOR
Ø18Ø 8192
152 EE
LOAD THE ADDRESS
INTO IOR AND THE
TU ADR REG.
152
7CØ1 FCØ1
MAINT MODE
14Ø FE
1 141
58ØØ 59A2
GO TO
1A2 GE
CPU CMDS ONLY
Ø 14Ø
SET OP-I
228Ø A2B4
174 AG
RAISE OP IN
MAINT CMND
QC115GD
174
SET TU SEL
Ø1ØØ 81ØE
14E BG
SELECT THE DRIVE
14E
GEN RST
Ø8CØ 88DC
15C DG
RESET ARLC
15C
RST GPC
Ø98Ø 898B
14B EG
14B
GT ADR-B-A
Ø4ØØ Ø43Ø
17Ø AK
17Ø
INCATE IOR
ØØCØ ØØF7
177 BK
LOAD THE TU ADR
BACK INTO IOR
FROM TU ADR REG.
1 177
R SENS CNTLS
3Ø8Ø BØB1
171 CK
RESET SENSE
CONTROLS TO
PERMIT S STA
CTL=7 ON QC121
TO WORK.
171
RST GT ADR-B
Ø44Ø 8475
175 EK
175
SET IOR-BI
2ØØØ A99D
15D FK
SEND ADR TO CHAN
QC121
MASTER
LOAD TU ADR REG
PRESENT E C 22Ø2Ø
DATE 6-25-73
CD LOC
CD PN
PREV E C 22Ø15
PG PN 31277
CD TYPE QC
MACH 38ØØ-111
QC111
20
QC111



SE	BUFFER COMMAND ACCESS			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31278	CD TYPE	MACH 38ØØ-111	


SEND ADR TO CHAN
QC111FK
SET DSE LTH
15D
2680 268D
14D ZA
1 14D
7201 7200
ADR-0
14C AB
WAIT FOR FALL OF ADR OUT
0 14C
SET ADR-I
2300 A308
148 BB
SET ADR-IN TAG
0 148
7400 7402
CMD-0
142 DB
WAIT FOR RISE OF COMMAND OUT TAG LINE
0 142
72C0 72C8
INTF DISC
148 EB
TEST FOR ADR OUT UP AND SELECT OUT DOWN
1 149
5800 583A
GO TO
03A FA
RETURN TO IDLE LOOP
QC105
1 143
ING CMDR, IOR
01C0 01C6
146 GB
PLACE THE COMMAND IN THE COMMAND REGISTER
AT LEAST 2 MICRO-SEC MUST BE ALLOWED BEFORE INTERROGATING TU STATUS LINES.
WTM-REW FROM SW'S
QS121GL
146
RST SEN, STAT
24C0 A4CA
14A ZD
NO RST IF CMD IS NOP, TIO, DGN SENSE OR THERE IS AN INTERRUPT PENDING
14A
S STA CTL=7
3040 B07B
17B AD
SET STATUS CONTROL LINES TO DRIVE ON.
17B
5800 5B90
GO TO
390 BD
1 385
RST ADR-I
2340 A352
392 BE
392
SET 30 CHK
2580 A583
383 CD
1 383
6100 E104
SEL TU BUSY
384 DD
0 384
7241 F247
INT PEND
386 ED
0 386
SET UC
0680 0689
389 FD
SEND FINAL STATUS
QC151DD
390
7181 71B5
BO P CHK
3B4 AF
0 3B4
RST ADR-I
2340 2342
382 BF
382
RST IOR-BI
28C0 A0D9
399 CF
399
RST NRDY
2B80 ABB1
3B1 DF
RESET THE FORCE NRDY CONDITION
1 385
SET BUSY
0580 0589
389 EF
1 387
SET BUSY
0580 0589
389 FF
1 389
5800 582D
GO TO
02D GF
SEND FINAL STATUS
QC191
DESIGN NOTE -- CANNOT RST ADR IN BEFORE TESTING FOR BUS-OUT PARITY CHECK, SINCE CHANNEL DROPS COMMAND CODE WHEN ADR IN FALLS, AND PARITY WILL BE BAD.
1 395
SET UC
0680 0689
389 FG
1 3B3
R SENS CNTLS
3080 3091
391 BH
SEE IF CAN LOOK AT OFFLINE SW
FOR CPU COMMANDS, TU OFFLINE SW MUST BE ONLINE
3B1
7C01 FC3B
MAINT MODE
3BA ZJ
0 3BA
6141 E173
SEL TU NRDY
3B2 AJ
0 3B2
7241 727F
INT PEND
3BE BJ
0 3BE
6401 E43D
TU OFF LINE
3BC CJ
1 3BD
FORCE NRDY
2BC0 ABD8
398 DJ
FORCE TU STAT A,B=0,1
398
6080 6094
NOT SENSE
394 EJ
TEST FOR STATUS
QC151
RESET STATUS CONTROL LINES TO DRIVE
TU NOT OFFLINE
QS101EL, QS11GC
1 38D
5800 DBCE
GO TO
3CE BK
1 3BF
R SENS CNTLS
3080 3091
391 CK
0 3BC
R SENS CNTLS
3080 3091
391 FK
391
5800 585F
GO TO
05F GK
CONTINUE CHECKING STATUS AND SENSE
QC131
TEST TAPE AT TI
QS111BD
1 3BB
6141 614D
SEL TU NRDY
3BC AL
CANNOT LOOK AT TU OFFLINE SW IF DRIVE IS NOT READY.
0 38C
6401 E401
TU OFFLINE
38D BL
FOR BUFFER COMMANDS, TU OFFLINE SWITCH MUST BE OFFLINE.
1 3B1
SET DATA MOD
1000 103C
3BC CL
0 38D
5800 DBCE
GO TO
3CE EL
3CE
SET STP LOOP
1840 9874
GO TO
3F4 FL
SET THE STOP LOOP TGR
MAINT OPERATION TU NOT OFFLINE
QC105
QC121
INITIAL SELECTION
PRESENT E C 22020
PREV E C 22015
DATE 6-25-73
PG PN 31279
CD LOC
CD TYPE
CD PN
MACH 3800-111
QC121


TIO STATUS
QC171
SET BUSY STATUS BIT
TEST THE BUSY LTH FOR THE SELECTED TU
TEST THE DRIVE 'NOT READY' LINE
SET THE BUSY LTH FOR THE SELECTED DRIVE
SEND FINAL STATUS
QC191
CONTINUE CHECKING STATUS AND SENSE
QC121GK
TIO ROUTINE ENTRY
RESET BUFFER CHAIN CONTROL
TEST FOR DE FOR SELECTED TU
TEST FOR PRESENCE OF MOD LINES
SEND FINAL STATUS
QC151
TEST FOR INT PENDING OR REM SHORT BUSY
SET BUSY STATUS
SET BUSY STATUS BIT
TEST FOR STATUS
QC151
TEST FOR PRESENCE OF MOD LINES
TEST THE DRIVE 'NOT READY' LINE
SET THE BUSY LTH FOR THE SELECTED DRIVE
CONT CMD DECODE
QC151
MOTION CONTROL CMDS
QC141
DSE, WRT, ERG, WTM, LWR
QC141
SET STATUS AND SENSE BITS
PRESENT E.C 22020
PREV E.C 22015
DATE 7-9-73
PG PN 31280
CD LOC
CD TYPE
CD PN
MACH 3800
QC1311

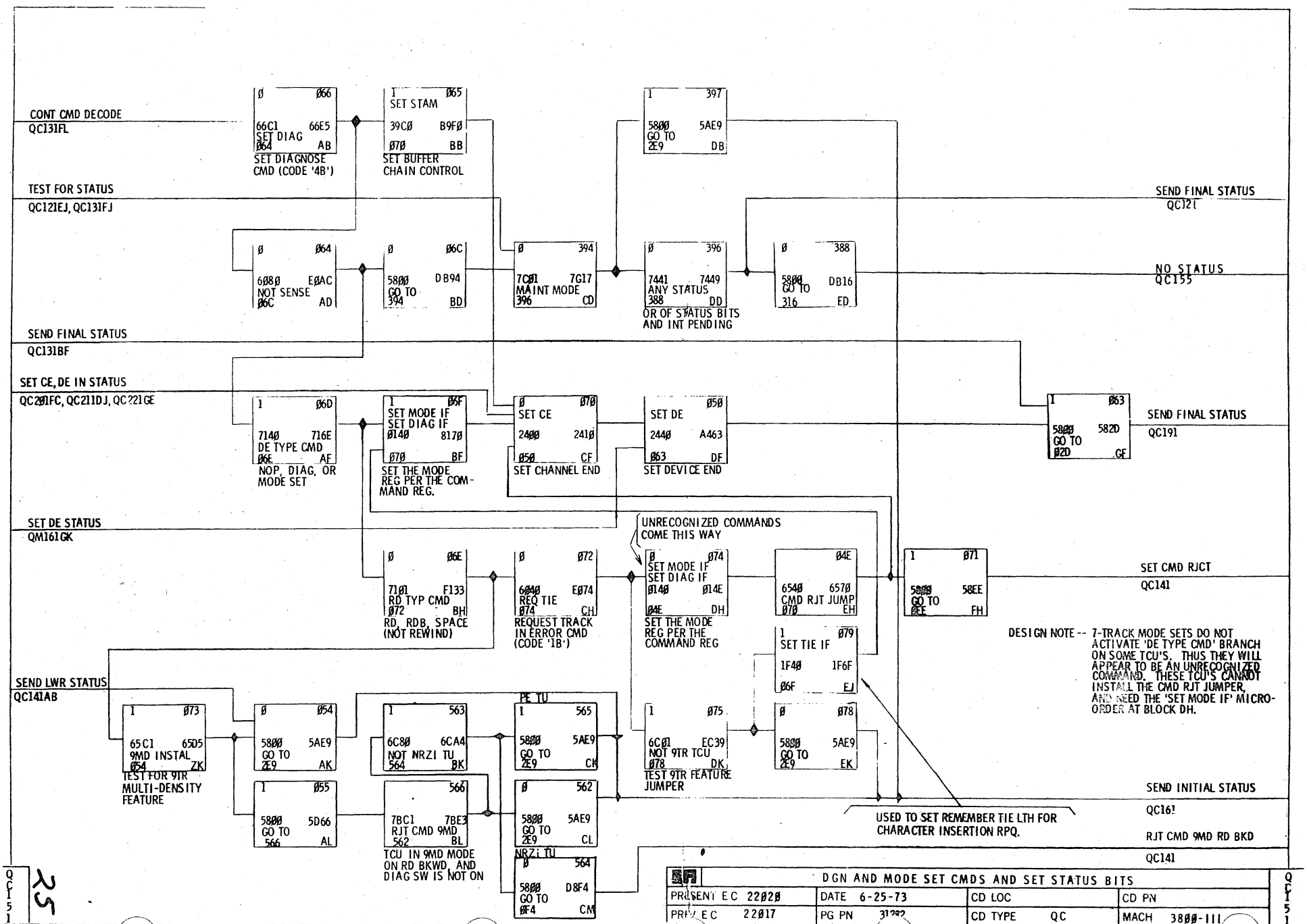


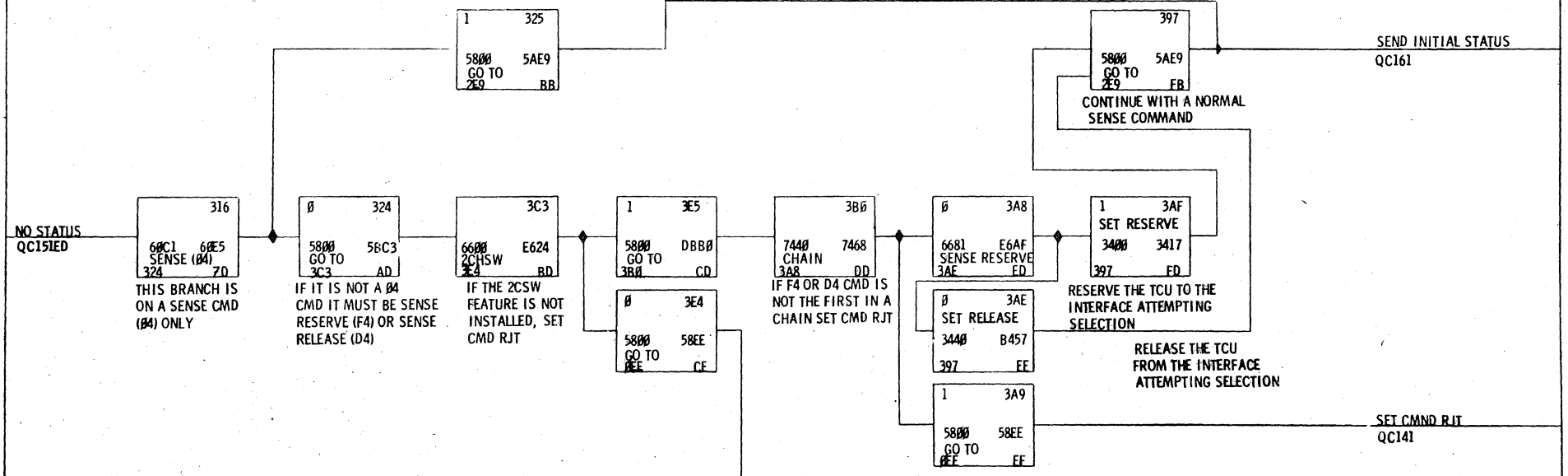
SET STATUS AND SENSE BITS FOR WRT & MOTION CMDS			
PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN
PREV EC 22017	PG PN 31281	CD TYPE	MACH 3800 - 111

QC141

24

QC141

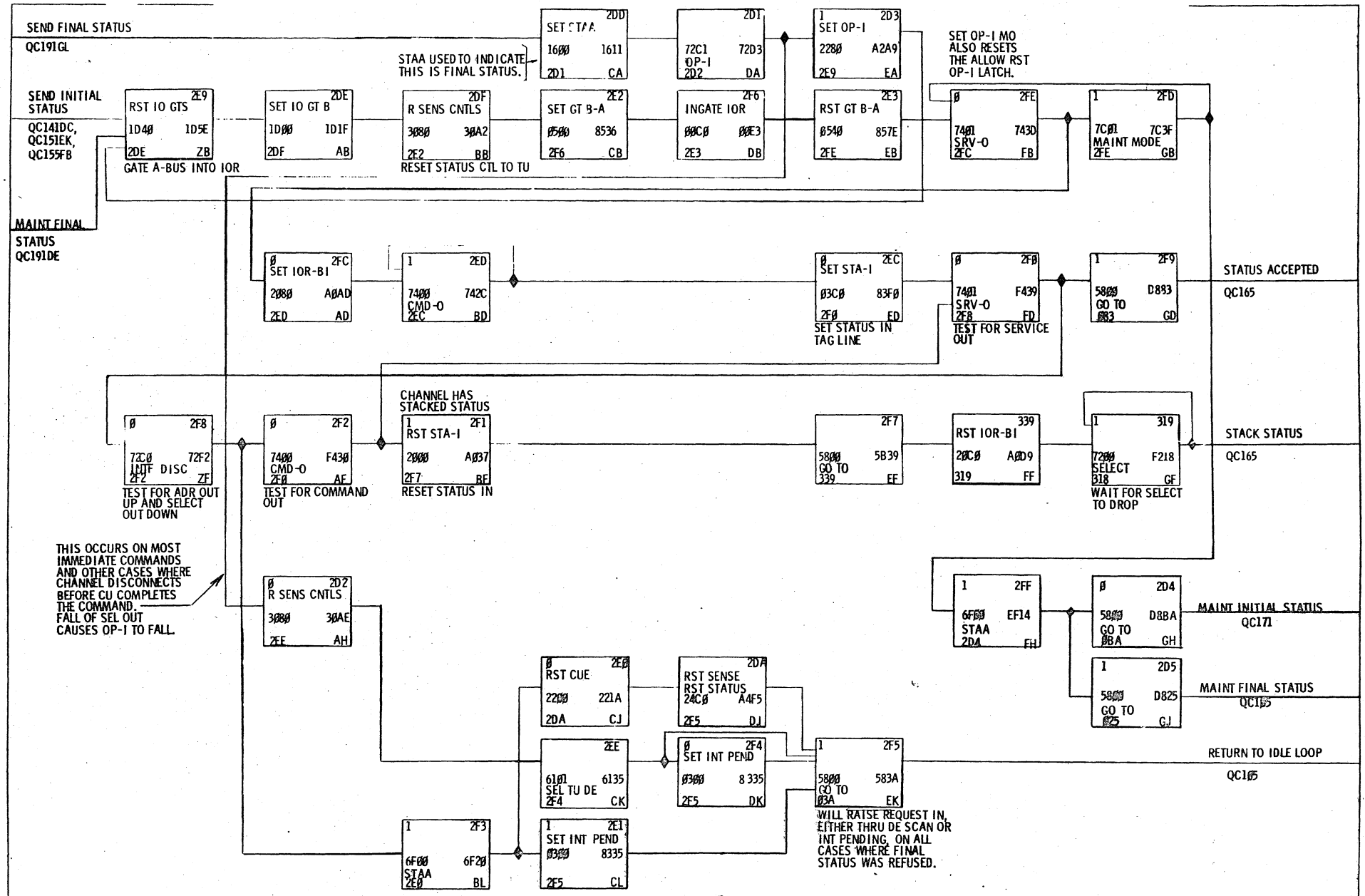

CONT CMD DECODE
QC131FL
TEST FOR STATUS
QC121EJ, QC131FJ
SEND FINAL STATUS
QC131BF
SET CE, DE IN STATUS
QC201FC, QC211DJ, QC221GE
SET DE STATUS
QM161GK
SEND LWR STATUS
QC141AB
SET DIAGNOSE CMD (CODE '4B')
SET BUFFER CHAIN CONTROL
OR OF STATUS BITS AND INT PENDING
SEND FINAL STATUS
QC121
NO STATUS
QC155
SEND FINAL STATUS
QC191
NOP, DIAG, OR MODE SET
SET THE MODE REG PER THE COMMAND REG.
SET CHANNEL END
SET DEVICE END
UNRECOGNIZED COMMANDS COME THIS WAY
RD, RDB, SPACE (NOT REWIND)
REQUEST TRACK IN ERROR CMD (CODE '1B')
SET THE MODE REG PER THE COMMAND REG
SET CMD RJCT
QC141
DESIGN NOTE -- 7-TRACK MODE SETS DO NOT ACTIVATE 'DE TYPE CMD' BRANCH ON SOME TCU'S. THUS THEY WILL APPEAR TO BE AN UNRECOGNIZED COMMAND. THESE TCU'S CANNOT INSTALL THE CMD RJT JUMPER, AND NEED THE 'SET MODE IF' MICRO-ORDER AT BLOCK DH.
TEST FOR 9TR MULTI-DENSITY FEATURE
TCU IN 9MD MODE ON RD BKWD AND DIAG SW IS NOT ON
TEST 9TR FEATURE JUMPER
USED TO SET REMEMBER TIE LTH FOR CHARACTER INSERTION RPQ.
SEND INITIAL STATUS
QC161
RJT CMD 9MD RD BKD
QC141
DGN AND MODE SET CMDS AND SET STATUS BITS
PRESENT EC 22Ø2Ø
DATE 6-25-73
CD LOC
CD PN
PRIV EC 22Ø17
PG PN 31282
CD TYPE QC
MACH 38ØØ-III
QC151
25
QC151



QC155 26

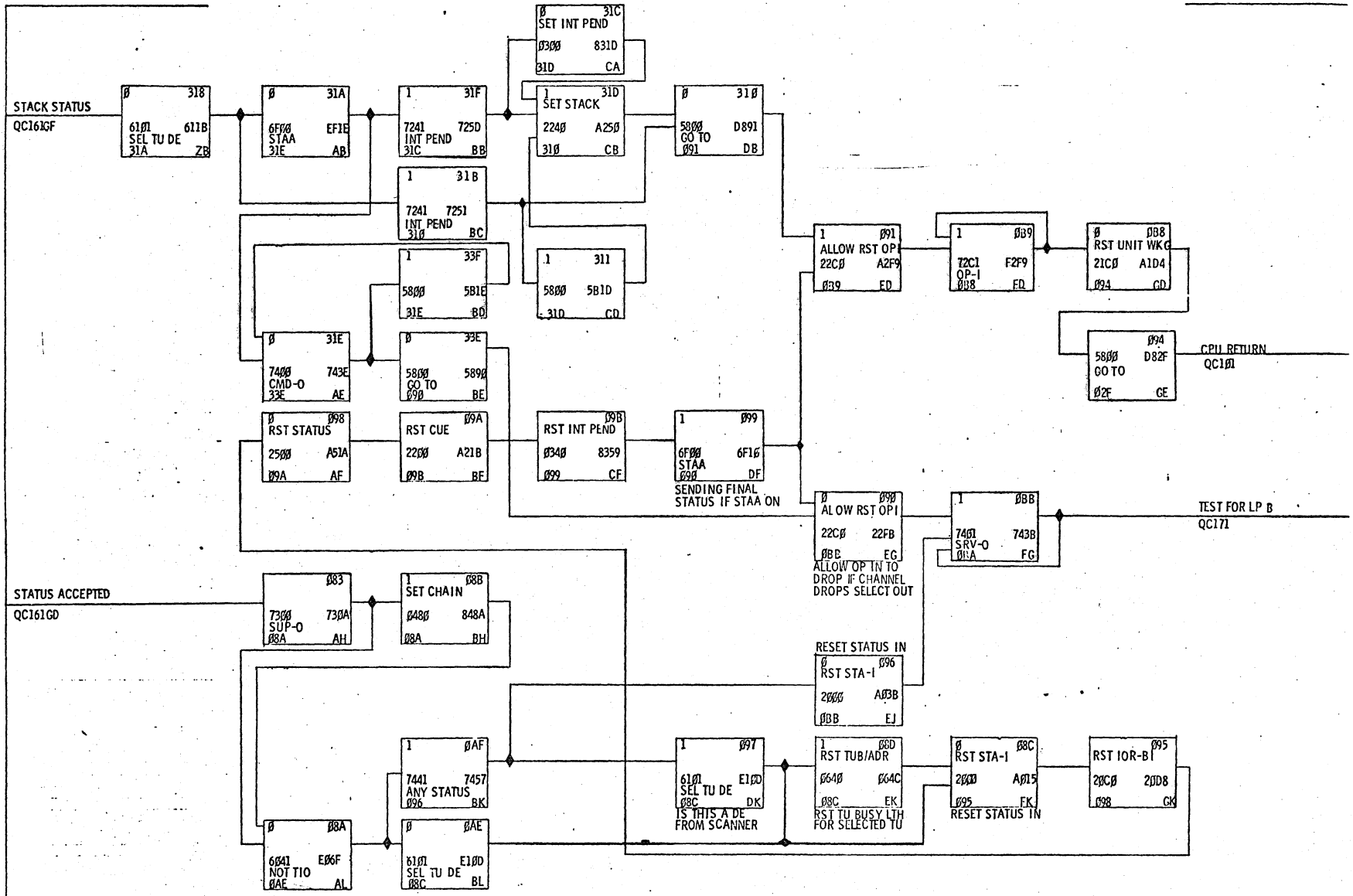
SENSE DECODING, SENSE RESERVE AND SENSE RELEASE			
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN
PREV E C 22017	PG PN 31283	CD TYPE	MACH

QC155



	SEND STATUS TO CHANNEL			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22Ø17	PG PN 31284	CD TYPE QC	MACH 38ØØ -	

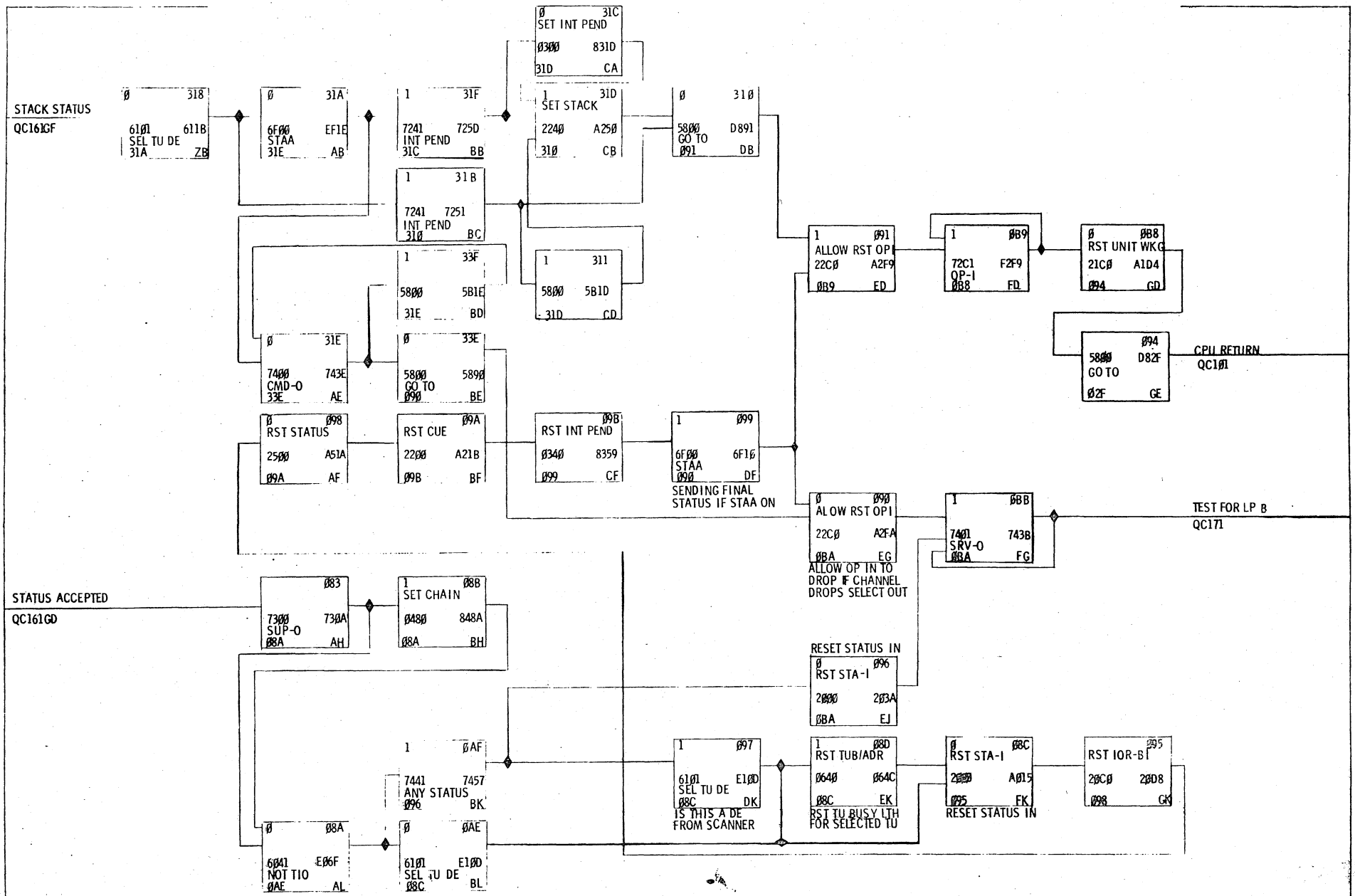
QC161 27 QC161



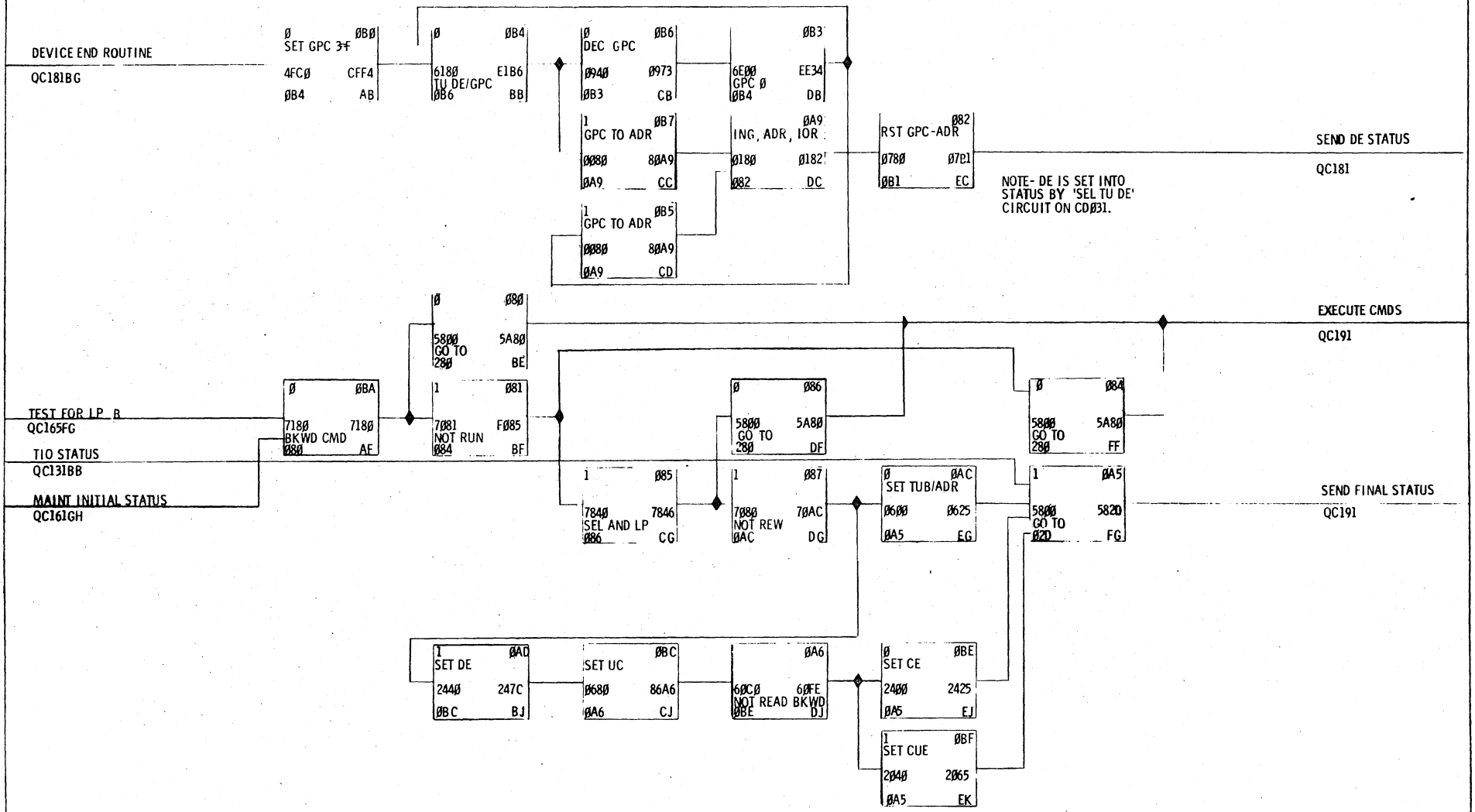
SEND STATUS TO CHANNEL				
PRESENT E C 22Ø21	DATE 1Ø/31/74	CD LOC	CD PN	
PREV E C 22Ø2Ø	PG PN 32Ø12 CD 7	CD TYPE QC	MACH 38ØØ-111	

QC165

QC165

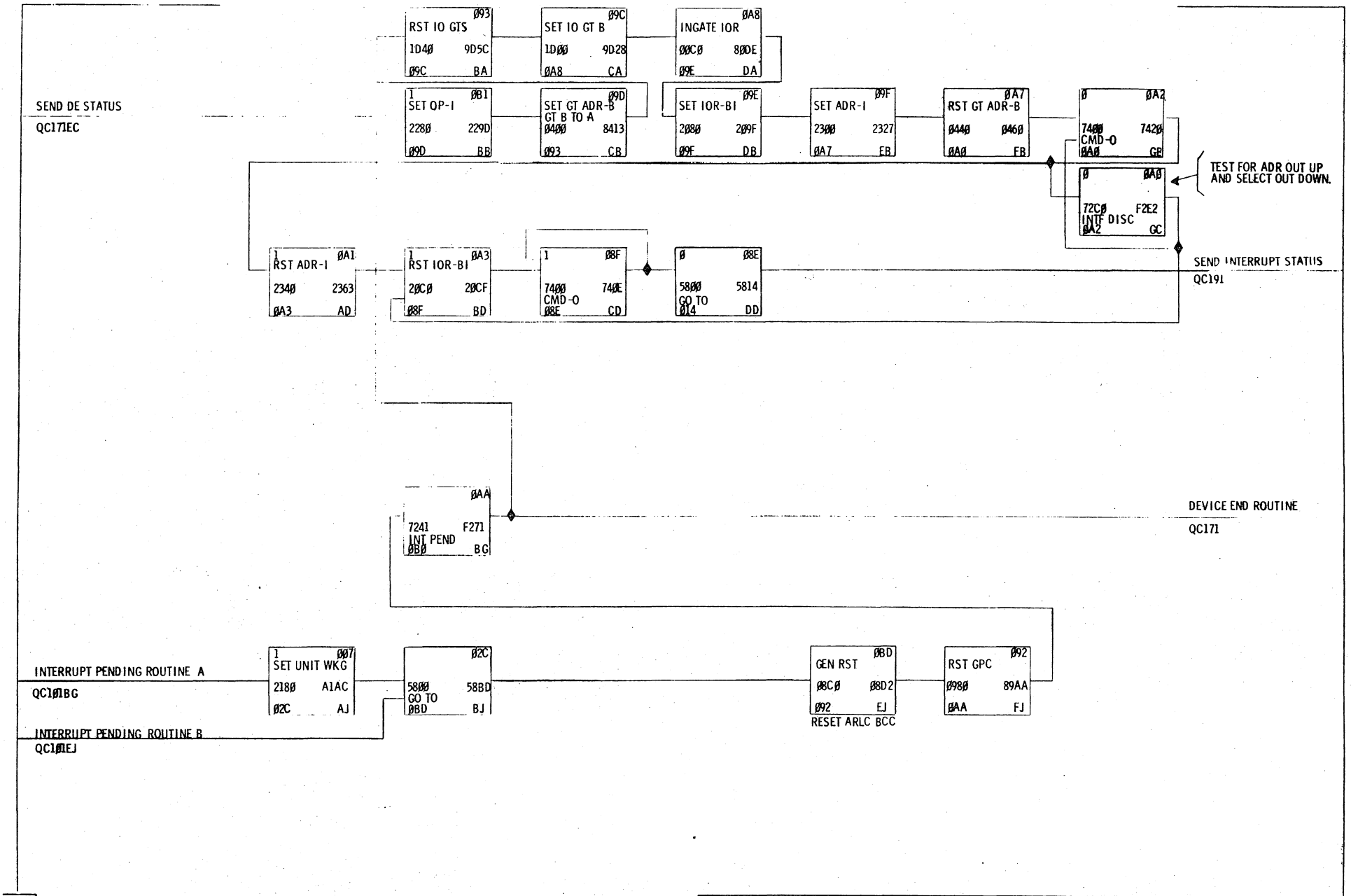


QC165	SEND STATUS TO CHANNEL				QC165
	PRESENT E C 22020	DATE 7-9-73	CD LOC	CD PN	
	PREV E C 22017	PG PN 31285	CD TYPE QC	MACH 3800-111	

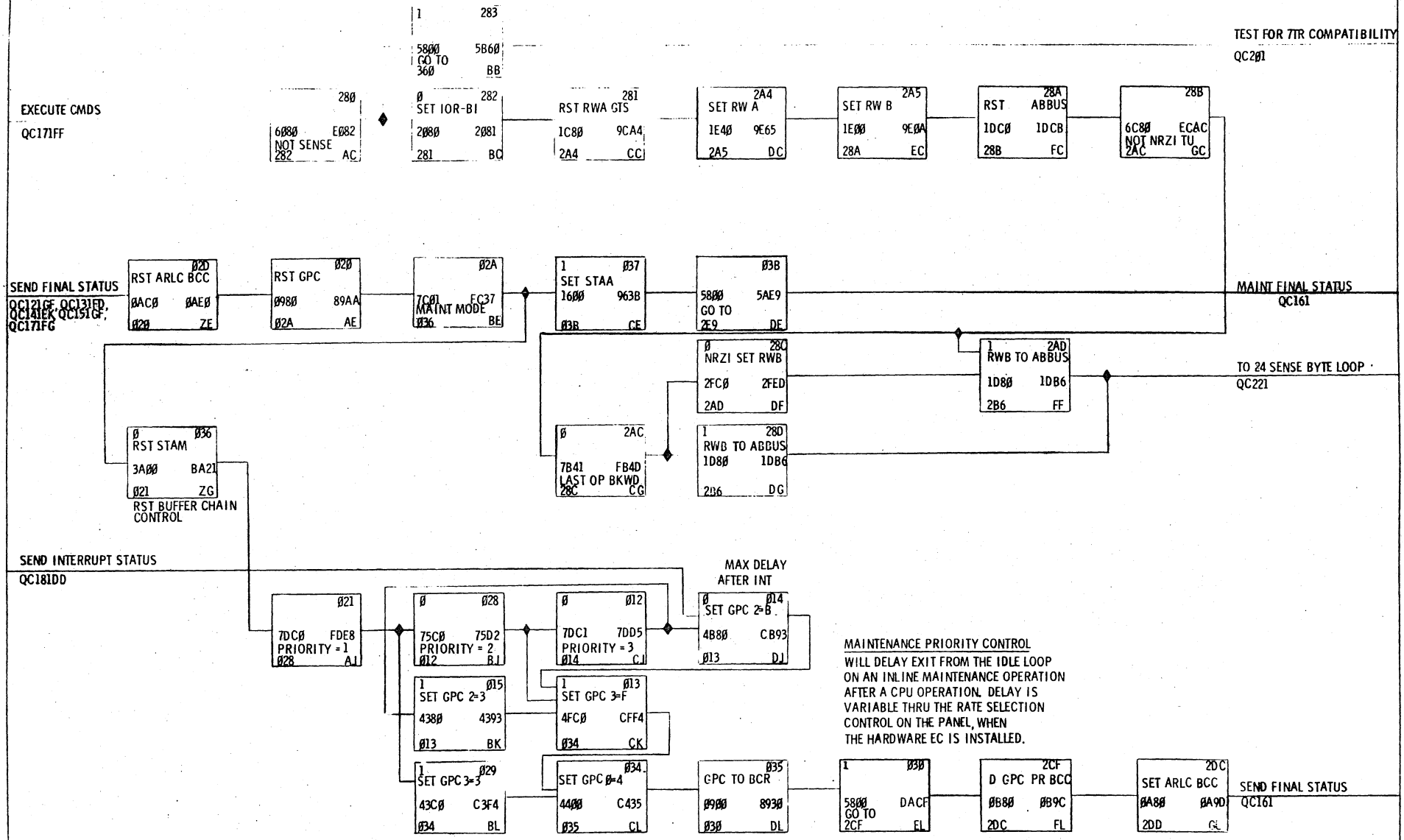


	DEVICE END SCANNER AND LP TEST			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31286	CD TYPE	MACH 38ØØ - 111	

QC171 30 QC171

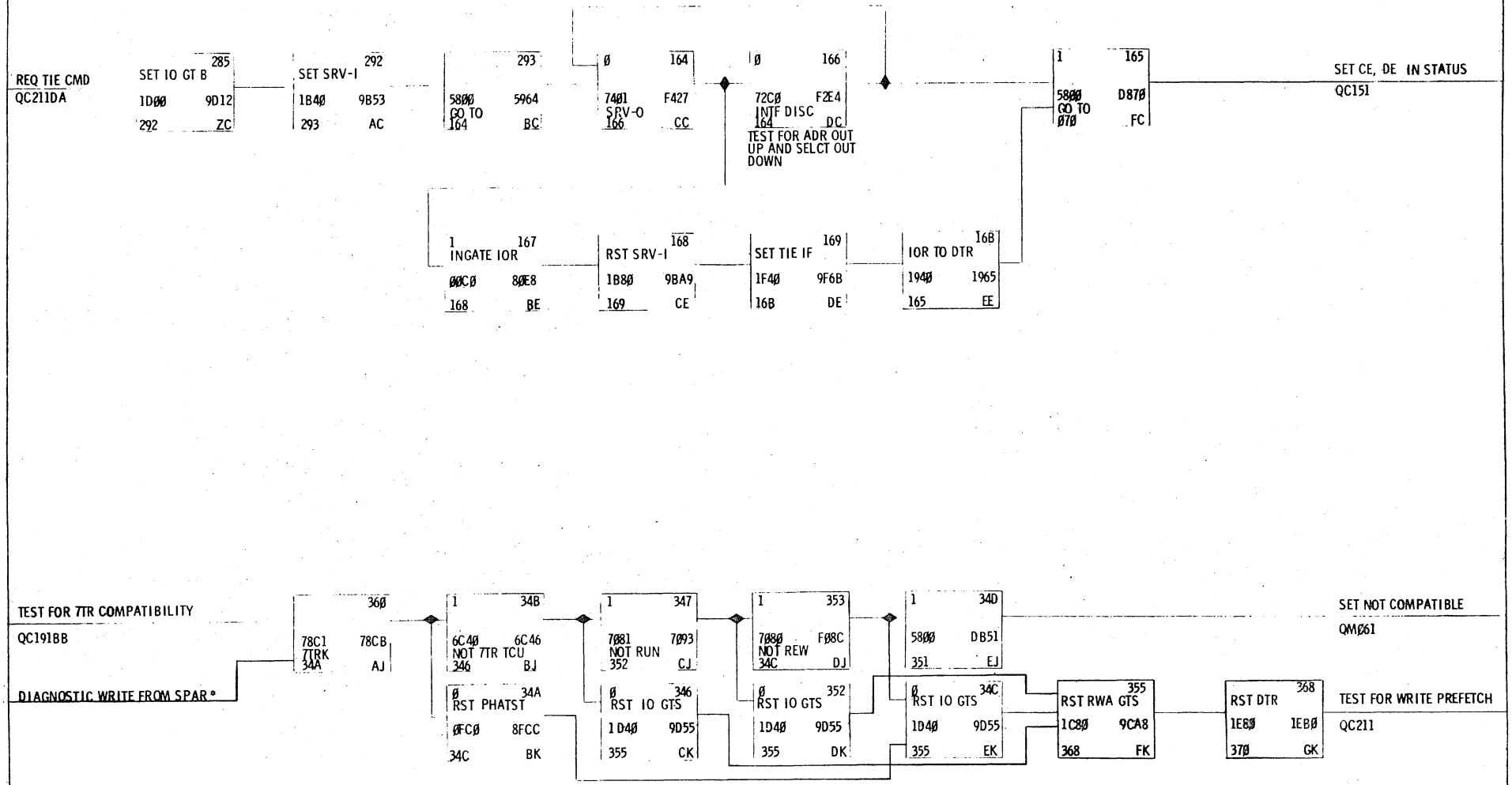


QC181	INTERRUPT PENDING ROUTINE			QC181
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22Ø15	PG PN 31287	CD TYPE	MACH 38ØØ - 111	



QC191	SENSE COMMAND AND PRIORITY CTL			QC191
PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22015	PG PN 31288	CD TYPE QC	MACH 3800 - 111	

32



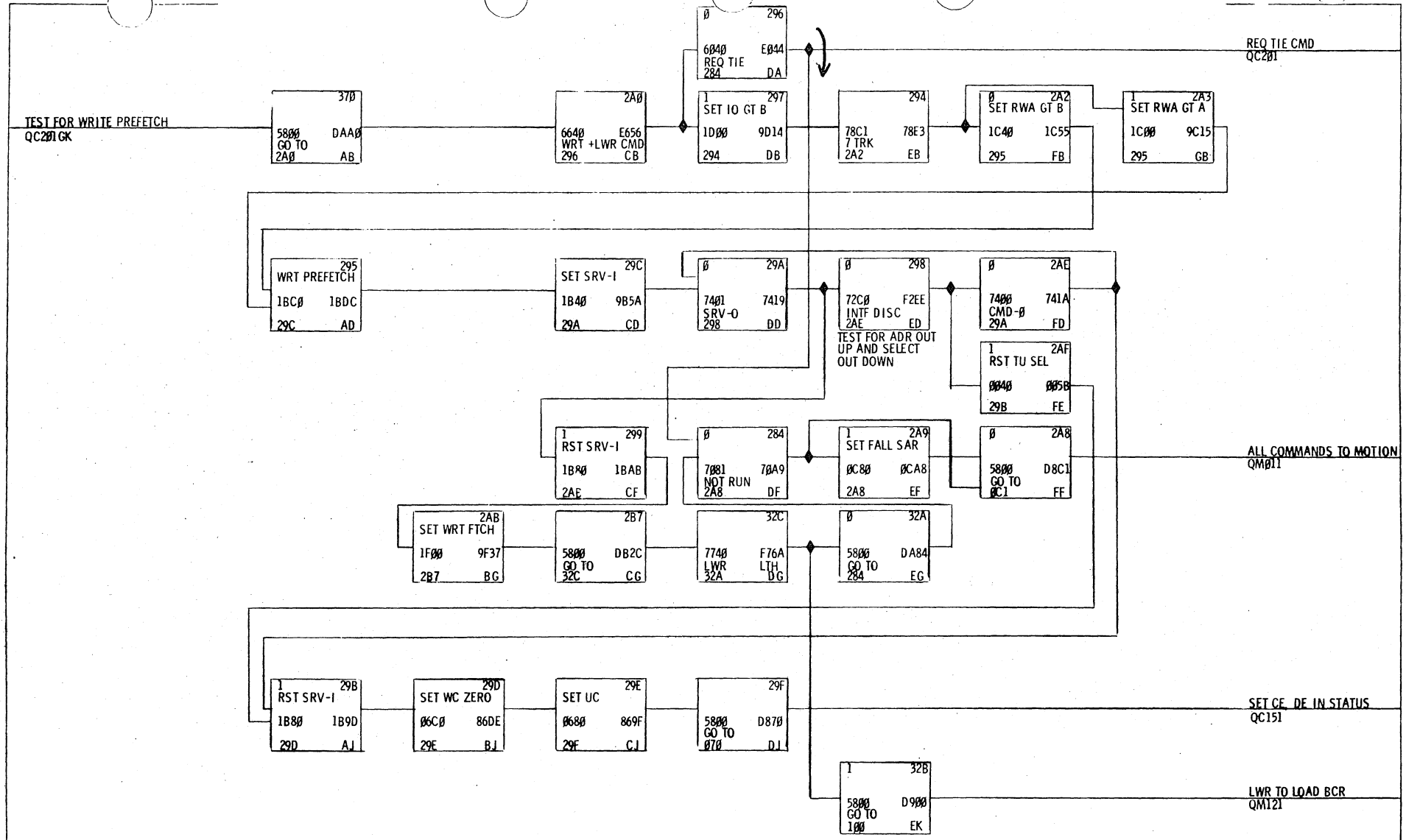
* ADDRESS 36Ø IS A RESERVED ENTRY TO THE MICRO-PROGRAM FROM SPAR FOR WRITING RECORDS FROM THE FE BUFFER IN DIAGNOSTIC MODE. BEFORE ENTRY, A DIAGNOSTIC MODE SET MUST BE SET IN THE MODE REG, STAS, STAM, AND GPC MUST BE RESET AND THE CHAIN TGR SET.

QC211

SW

REQ TI COMMAND			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C 22Ø15	PG PN 31289	CD TYPE	MACH 38ØØ - 111

QC211

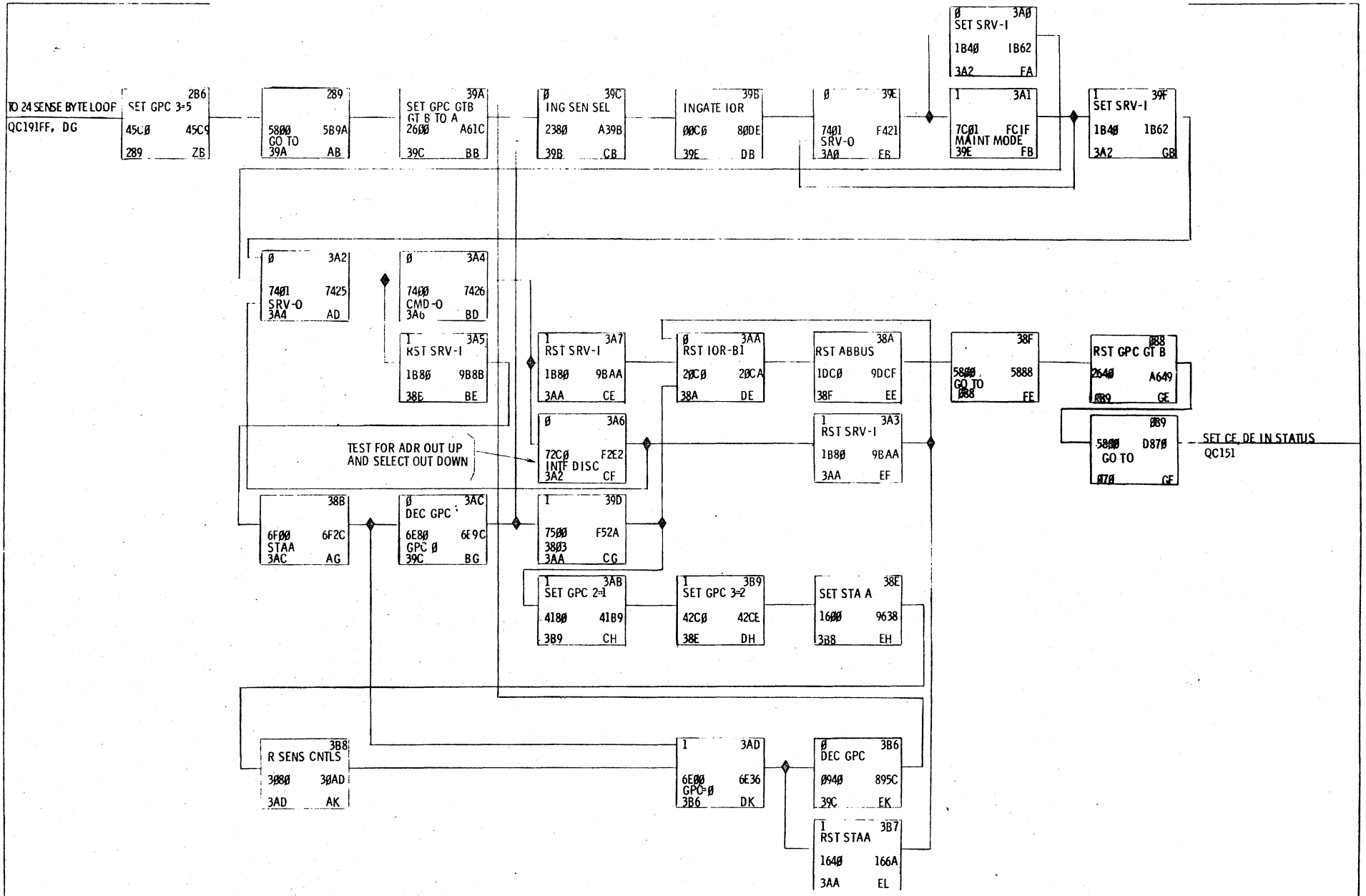


WRITE PREFETCH				
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31345	CD TYPE	MACH 38ØØ-III	

QC211

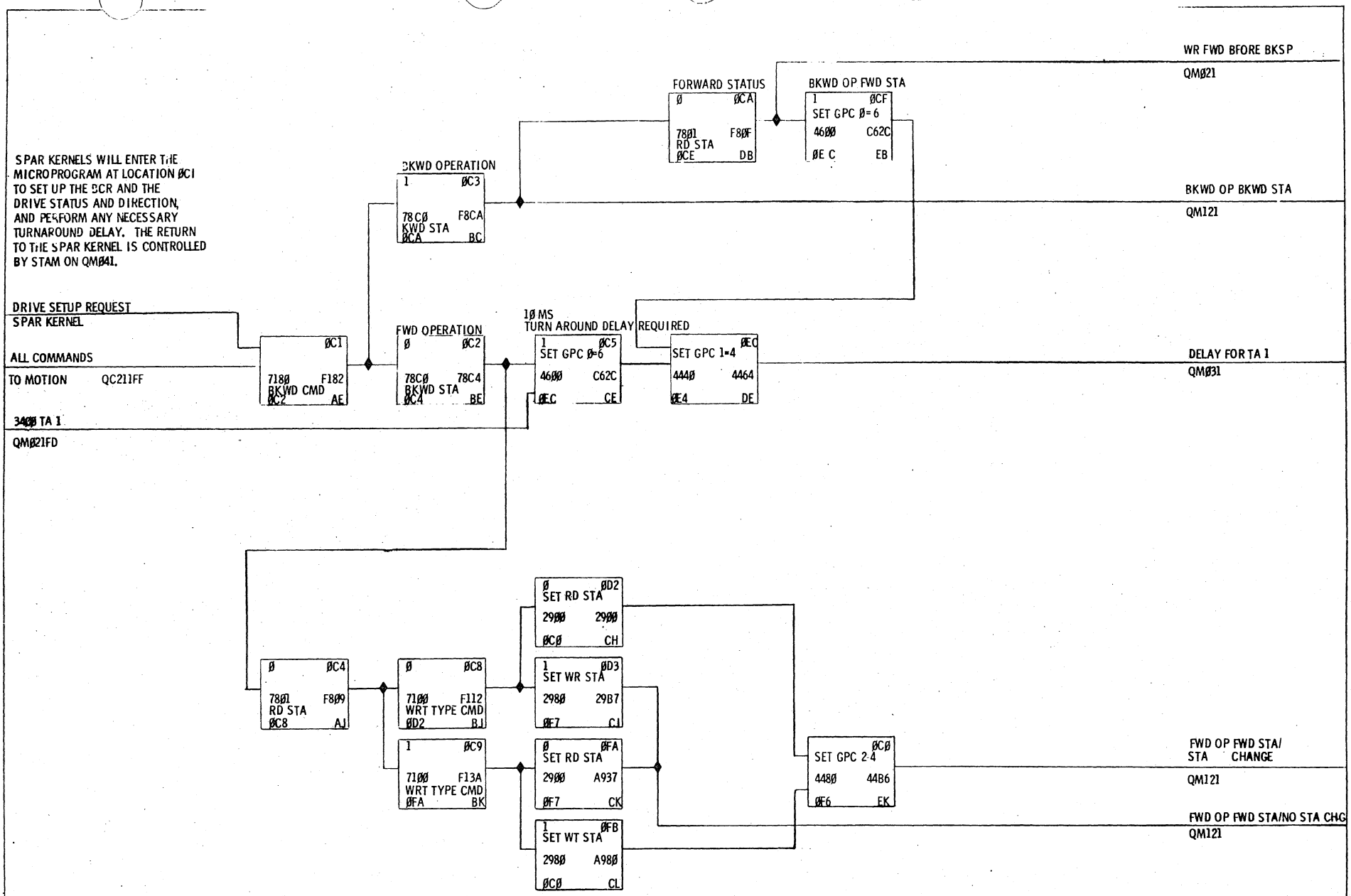
34

QC211

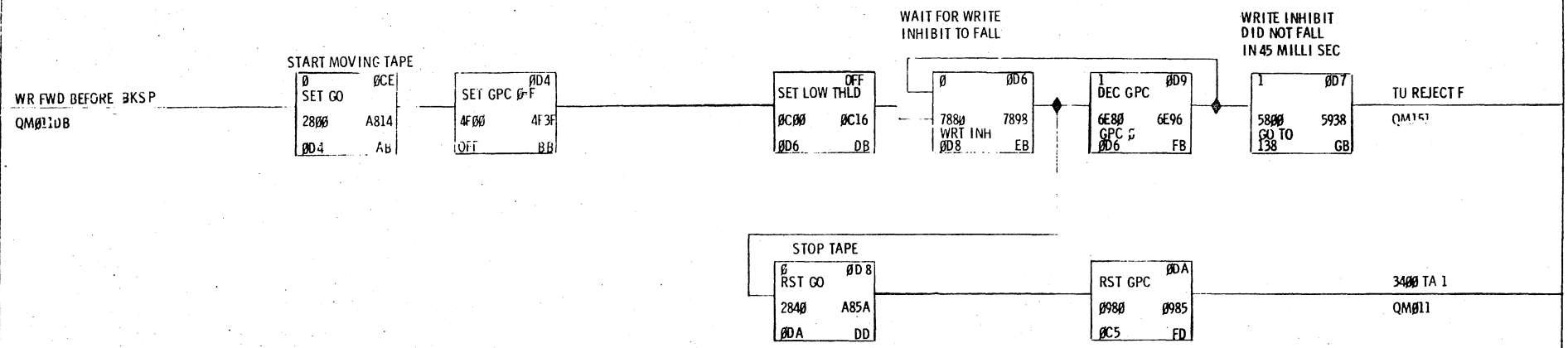


24 SENSE BYTE LOOP (NEW CE CARD)			
PRESENT EC 22Ø2Ø	DATE 7-9-73	CD LOC	CD PN
PREV EC 22Ø15	PG PN 31[illegible]	CD TYPE	MACH 38ØØ-III

QC221 35 QC221



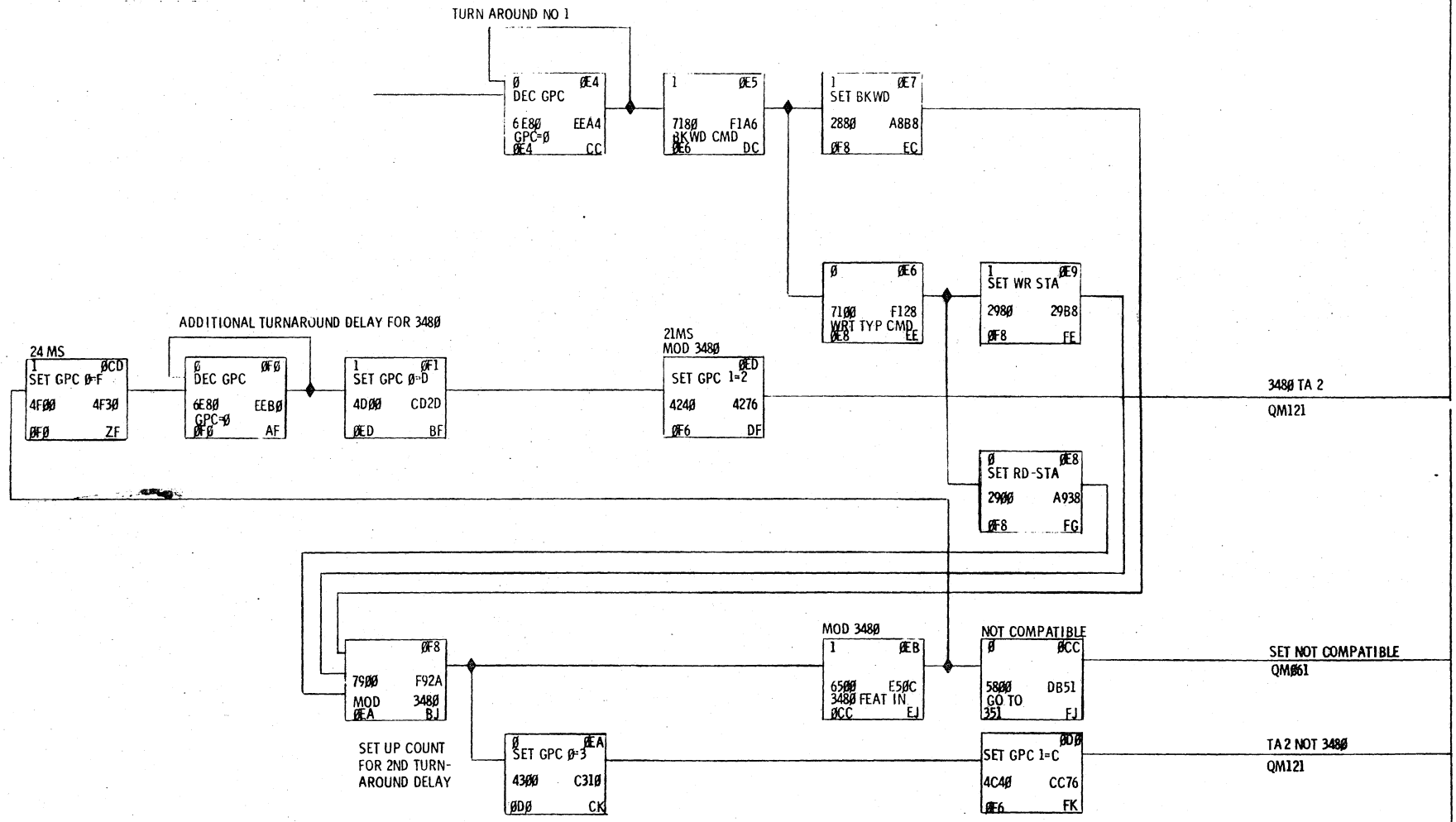
QMØ11	MOTION - INITIAL ENTRY			QMØ11
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22015	PG PN 31291	CD TYPE QM	MACH 3800 - 111	



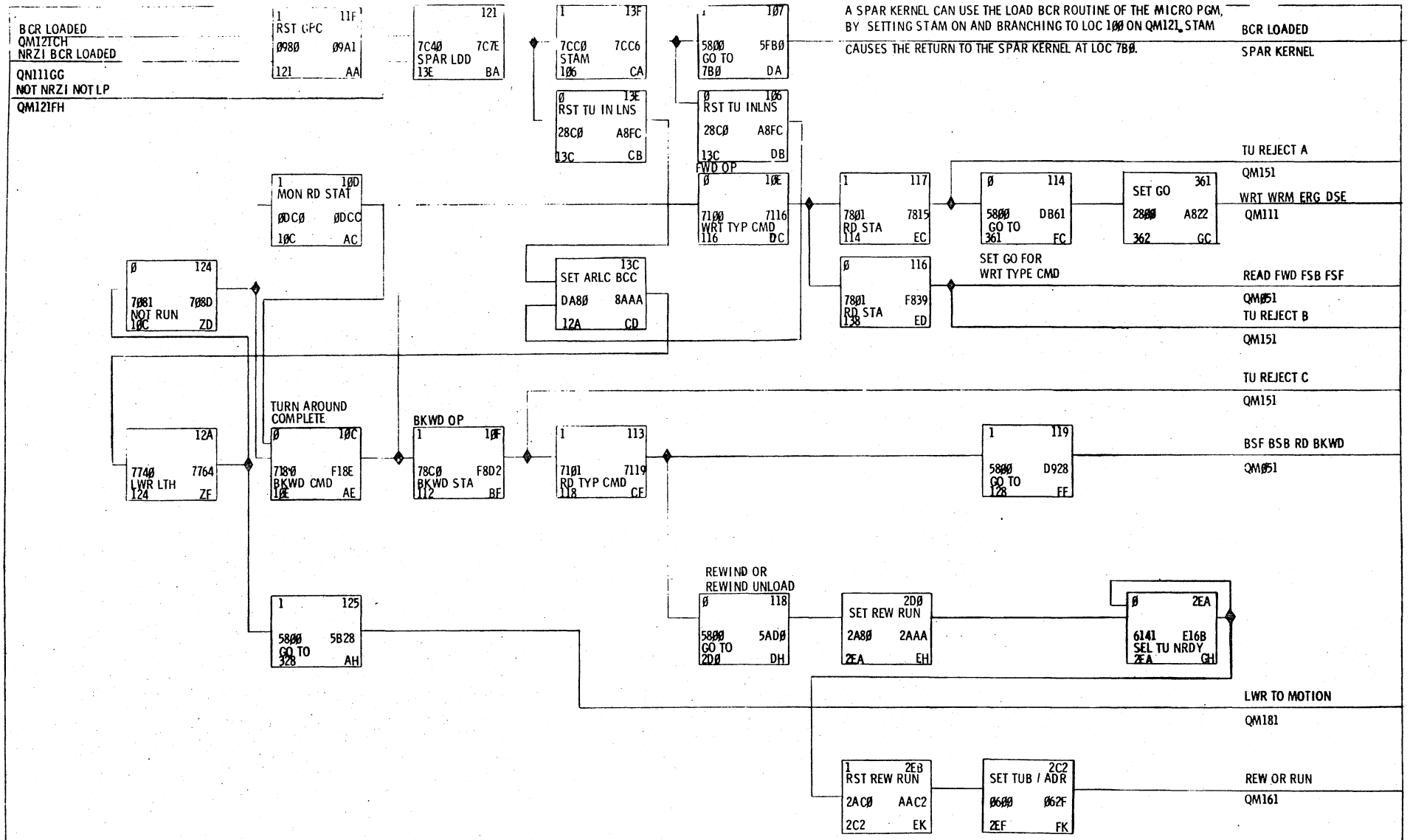
IF A BACKSPACE COMMAND FOLLOWS A WRITE COMMAND, THE TAPE IS MOVED FORWARD IN WRITE STATUS UNTIL WRT INHIBIT FALLS BEFORE BEGINNING THE BACKSPACE OPERATION. THIS ASSURES A PROPER GAP AFTER THE PREVIOUSLY WRITTEN RECORD.

WR BEFORE BACKSPACE - FORWARD HITCH				QMØ21
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø17	PG PN 31292	CD TYPE QM	MACH 38ØØ - III	

DELAY FOR TA 1
QMØ11DE

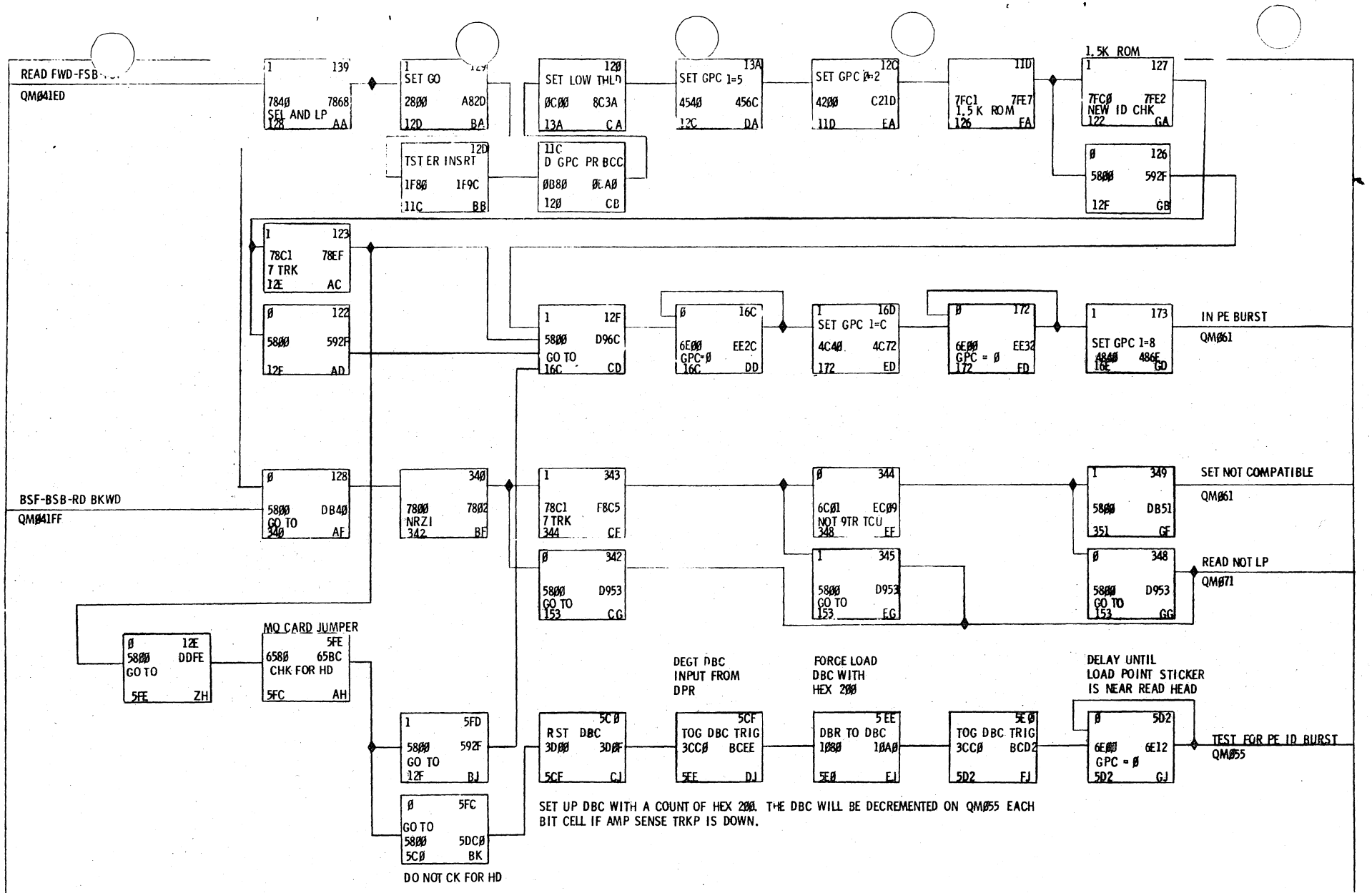


QMØ31	38	TURNAROUND		QMØ31
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31293	CD TYPE QM	MACH 38ØØ - 111	



	COMMAND DECODING			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22Ø15	PG PN 31294	CD TYPE	MACH 38ØØ - 111	

QM041

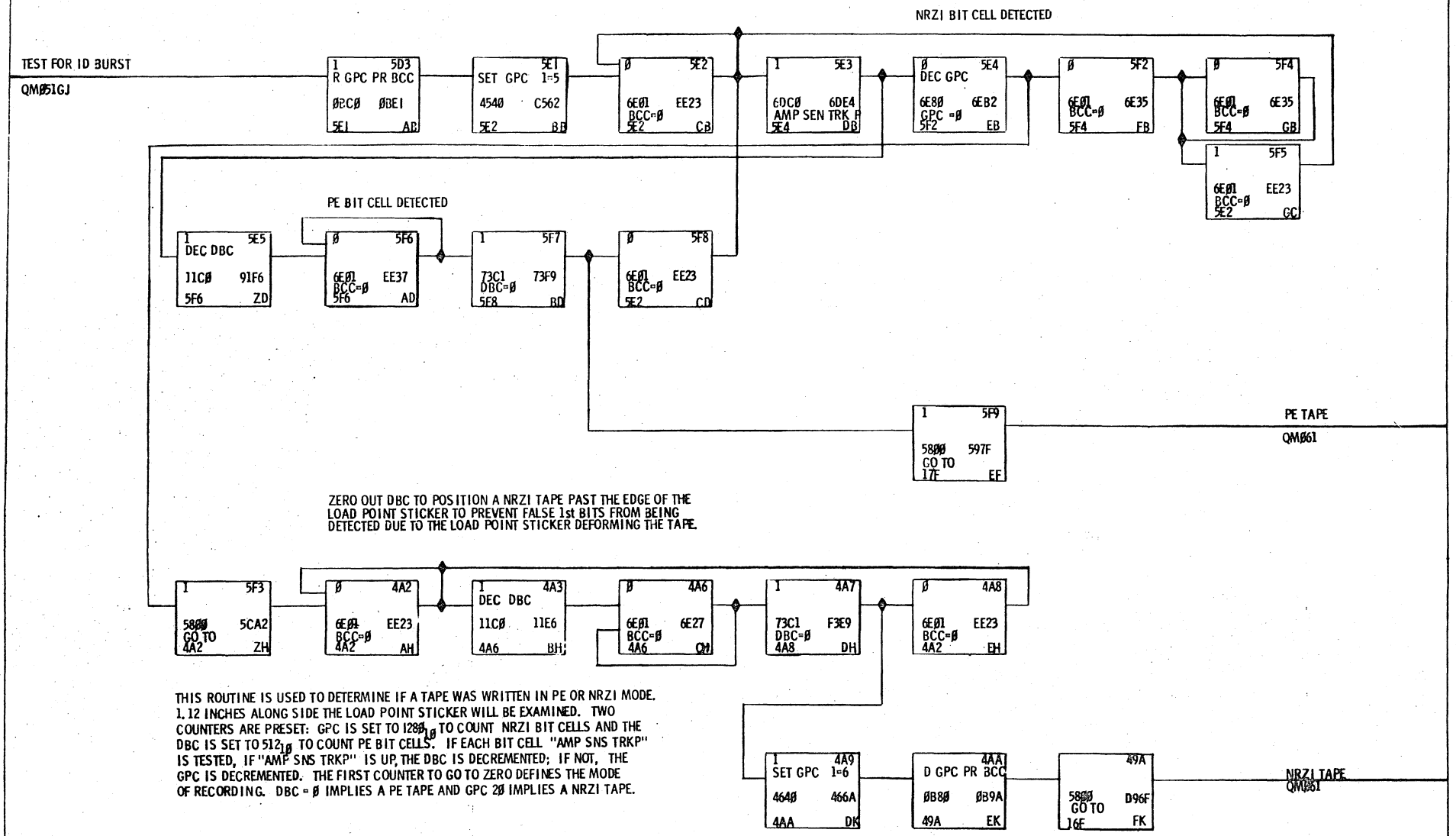


QM051 04

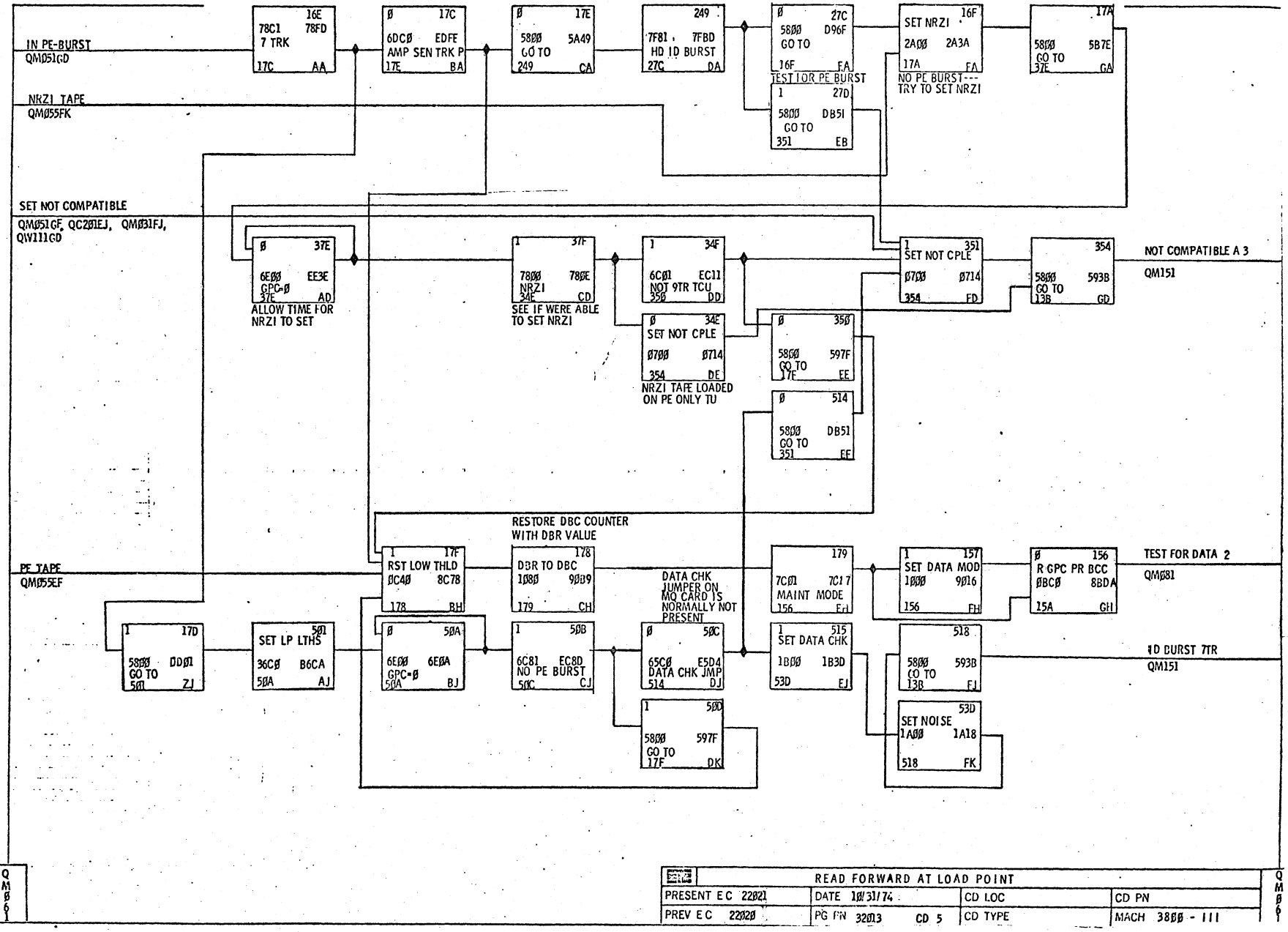
MASTER

READ FORWARD AT LOAD POINT			
PRESENT EC 22020	DATE 7-9-73	CD LOC	CD PN
PREV EC 22015	PG PN 31295	CD TYPE	MACH 3800 - 111

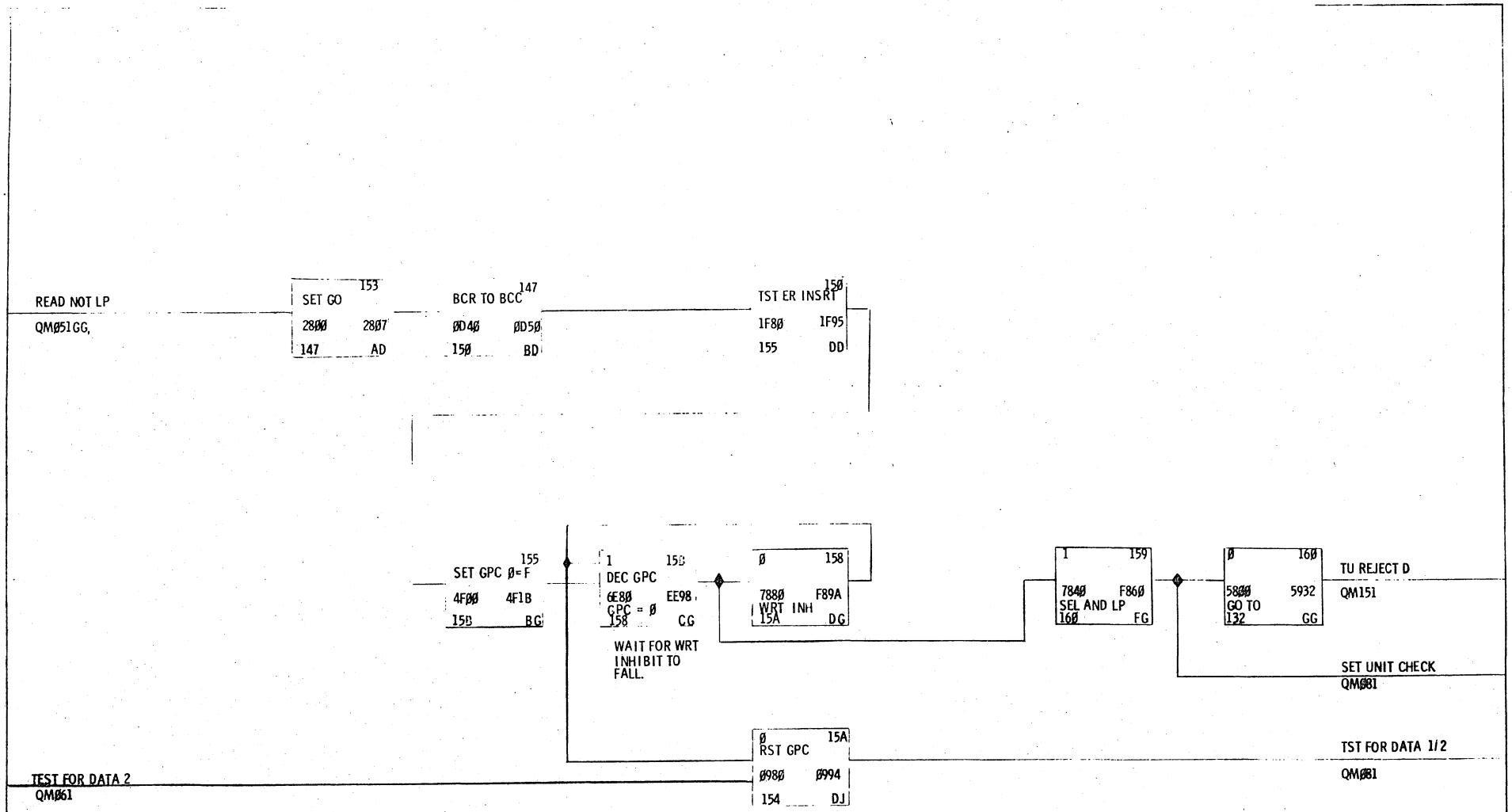
QM051



ID BURST DETECTION (SAMPLING TECH)			
PRESENT E C 22Ø2Ø	DATE 7-9-73	CD LOC	CD PN
PREV E C	PG PN 31296	CD TYPE QM	MACH


IN PE-BURST
QMØ51GD
NRZI TAPE
QMØ55FK
SET NOT COMPATIBLE
QMØ51GF, QC2Ø1EJ, QMØ31FJ, QW111GD
PE TAPE
QMØ55EF
16E 78C1 78FD 7 TRK 17C AA
Ø 17C 6DCØ EDFE AMP SEN TRK P 17E BA
Ø 17E 58ØØ 5A49 GO TO 249 CA
249 7F81 7FBD HD ID BURST 27C DA
Ø 27C 58ØØ D96F GO TO 16F FA
TEST FOR PE BURST
1 27D 58ØØ DB51 GO TO 351 EB
SET NRZI 16F 2AØØ 2A3A 17A FA
NO PE BURST--- TRY TO SET NRZI
17A 58ØØ 5B7E GO TO 37E GA
Ø 37E 6EØØ EE3E GPC-Ø 37E AD
ALLOW TIME FOR NRZI TO SET
1 37F 78ØØ 78ØE NRZI 34E CD
SEE IF WERE ABLE TO SET NRZI
1 34F 6CØ1 EC11 NOT 9TR TCU 35Ø DD
Ø 34E SET NOT CPLE Ø7ØØ Ø714 354 DE
NRZI TAPE LOADED ON PE ONLY TU
1 351 SET NOT CPLE Ø7ØØ Ø714 354 FD
354 58ØØ 593B GO TO 13B GD
NOT COMPATIBLE A 3
QM151
Ø 35Ø 58ØØ 597F GO TO 17E EE
Ø 514 58ØØ DB51 GO TO 351 EE
RESTORE DBC COUNTER WITH DBR VALUE
1 17F RST LOW THLD ØC4Ø 8C78 178 BH
178 DBR TO DBC 1Ø8Ø 9ØB9 179 CH
DATA CHK JUMPER ON MQ CARD IS NORMALLY NOT PRESENT
179 7CØ1 7C17 MAINT MODE 156 FH
1 157 SET DATA MOD 1ØØØ 9Ø16 156 FH
Ø 156 R GPC PR BCC ØBCØ 8BDA 15A GH
TEST FOR DATA 2
QMØ81
1 17D 58ØØ DDØ1 GO TO 5Ø1 ZJ
5Ø1 SET LP LTHS 36CØ B6CA 5ØA AJ
Ø 5ØA 6EØØ 6EØA GPC-Ø 5ØA BJ
1 5ØB 6C81 EC8D NO PE BURST 5ØC CJ
Ø 5ØC 65CØ E5D4 DATA CHK JMP 514 DJ
1 5ØD 58ØØ 597F GO TO 17E DK
1 515 SET DATA CHK 1BØØ 1B3D 53D EJ
518 58ØØ 593B GO TO 13B FJ
ID BURST 7TR
QM151
53D SET NOISE 1AØØ 1A18 518 FK
QMB61
READ FORWARD AT LOAD POINT
PRESENT E C 22Ø21
DATE 1Ø/31/74
CD LOC
CD PN
PREV E C 22Ø2Ø
PG PN 32Ø13
CD 5
CD TYPE
MACH 38ØØ - 111
QMB61

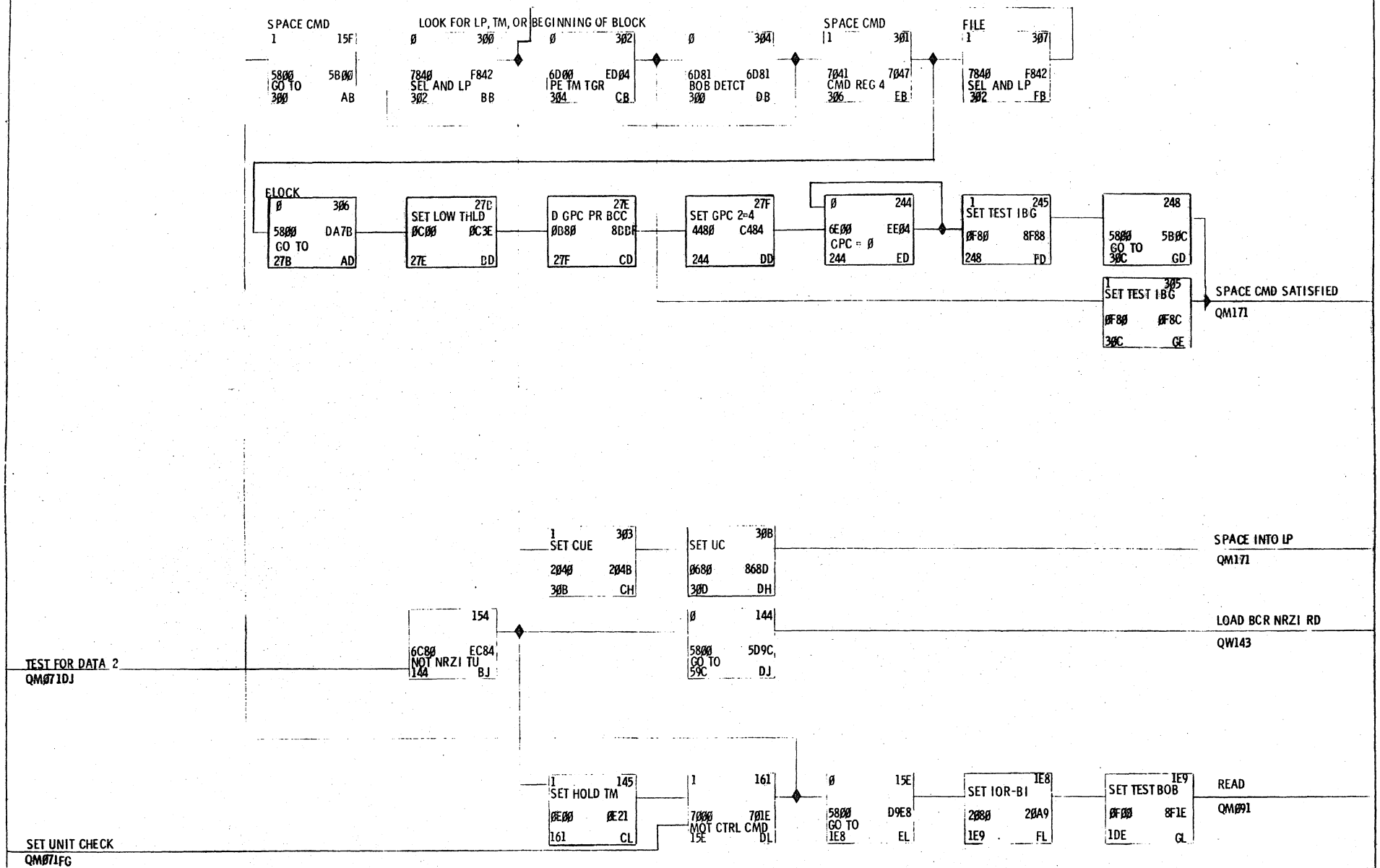
42



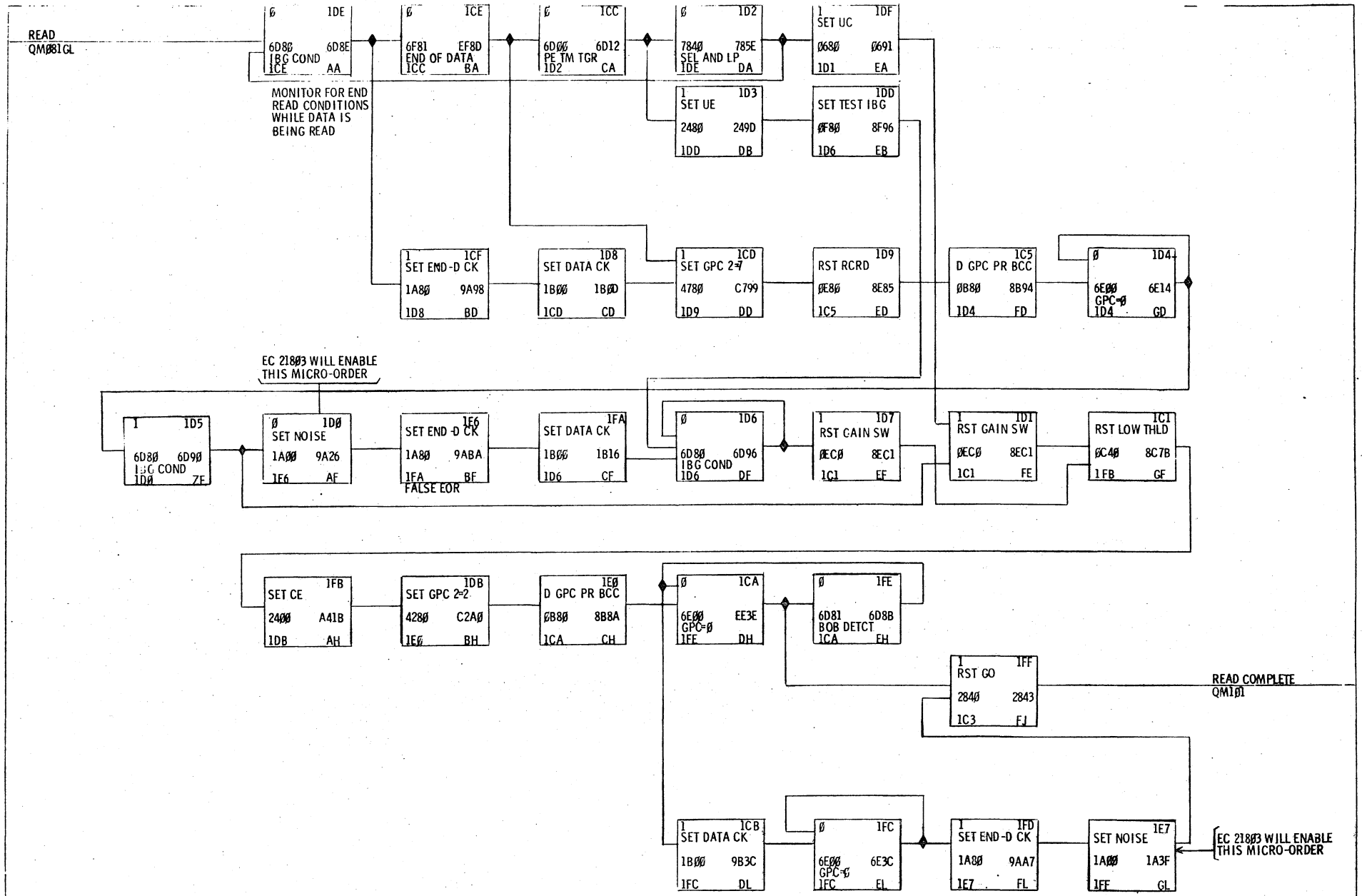
READ NOT AT LOAD POINT			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C 22Ø15	PG PN 31298	CD TYPE	MACH 38ØØ - 111

QM071

43



QM081	TEST FOR BOB OR TM			QM081
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22015	PG PN 31299	CD TYPE	MACH 3800 - 111	



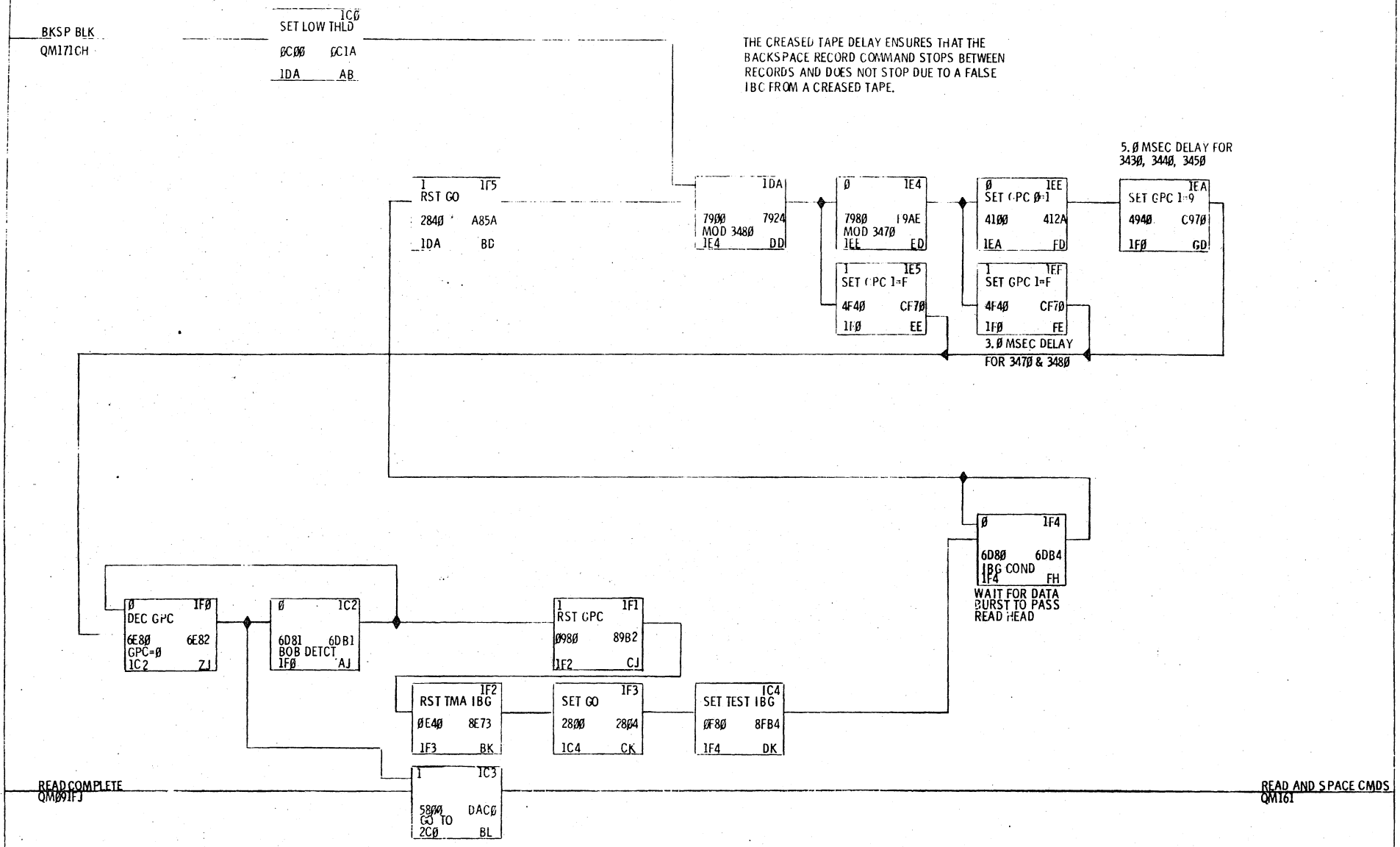
QM Ø 1

415

END READ SENSE FOR IBG

PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C 2201[illegible]	PG PN 313ØØ	CD TYPE	MACH 38ØØ-111

QM Ø 9 1

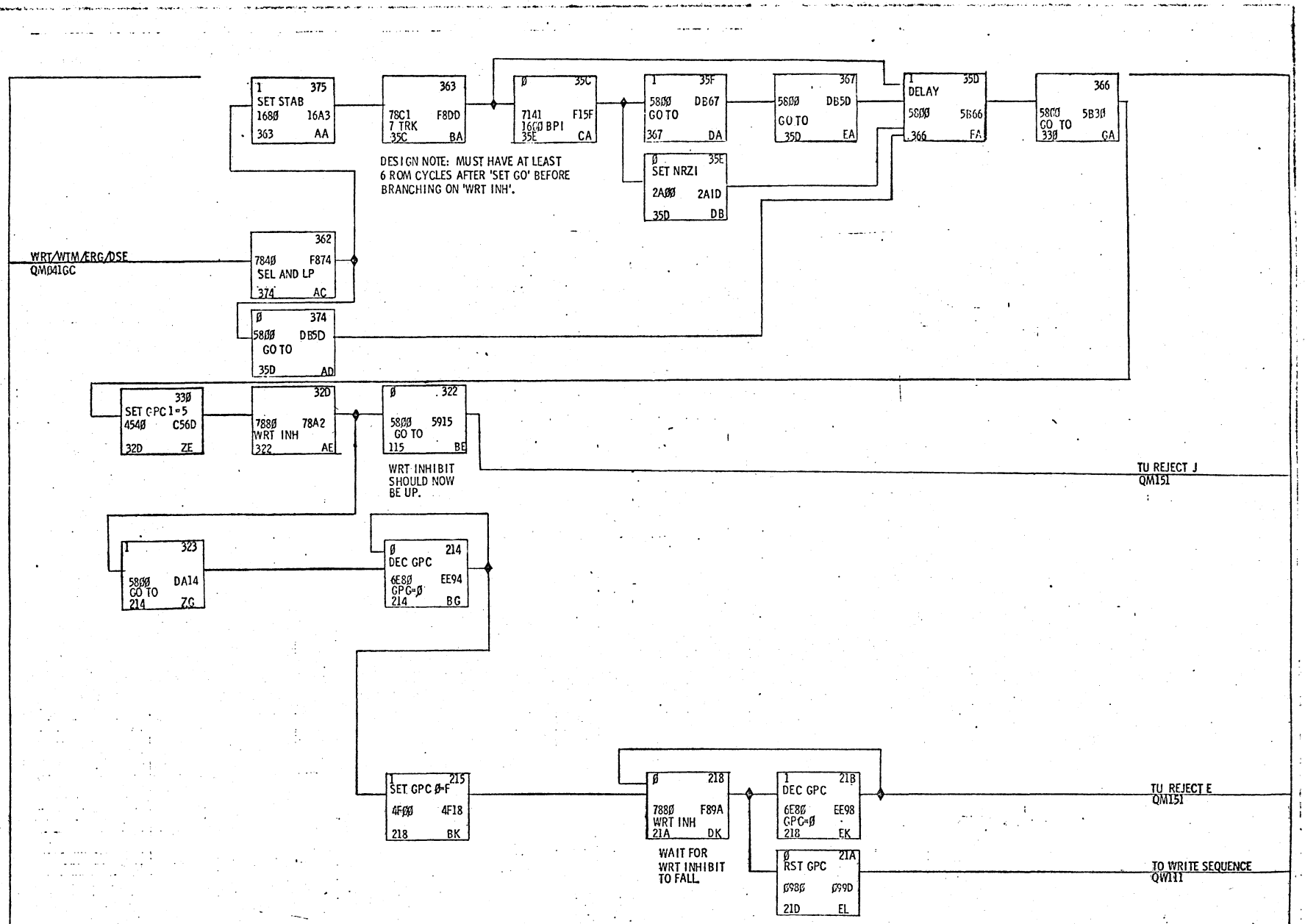


	CREASED TAPE DELAY ON BACKSPACE BLOCK			
PRESENT E C 22Ø26	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31301	CD TYPE	MACH 38ØØ-111	

QM191

94

QM191


1 375
SET STAB
168Ø 16A3
363 AA
363
78C1 F8DD
7 TRK
35C BA
Ø 35C
7141 F15F
1600 BPI
35E CA
1 35F
58ØØ DB67
GO TO
367 DA
367
58ØØ DB5D
GO TO
35D EA
1 35D
DELAY
58ØØ 5B66
366 FA
366
58ØØ 5B3Ø
GO TO
33Ø GA
DESIGN NOTE: MUST HAVE AT LEAST
6 ROM CYCLES AFTER 'SET GO' BEFORE
BRANCHING ON 'WRT INH'.
Ø 35E
SET NRZI
2AØØ 2AID
35D DB
WRT/WTM/ERG/DSE
QMØ41GC
362
784Ø F874
SEL AND LP
374 AC
Ø 374
58ØØ DB5D
GO TO
35D AD
33Ø
SET GPC 1-5
454Ø C56D
32D ZE
32D
788Ø 78A2
WRT INH
322 AE
Ø 322
58ØØ 5915
GO TO
115 BE
WRT INHIBIT
SHOULD NOW
BE UP.
TU REJECT J
QM151
1 323
58ØØ DA14
GO TO
214 ZG
Ø 214
DEC GPC
6E8Ø EE94
GPC=Ø
214 BG
1 215
SET GPC Ø-F
4FØØ 4F18
218 BK
Ø 218
788Ø F89A
WRT INH
21A DK
WAIT FOR
WRT INHIBIT
TO FALL
1 21B
DEC GPC
6E8Ø EE98
GPC=Ø
218 EK
TU REJECT E
QM151
Ø 21A
RST GPC
Ø98Ø Ø99D
21D EL
TO WRITE SEQUENCE
QW111
BEGINNING OF WRITE
PRESENT E.C. 22Ø21
DATE 1Ø/31/74
CD LOC
CD PN
PREV E.C. 22Ø2Ø
32Ø14 CD 3
CD TYPE
MACH 38Ø
Q M
Q M I

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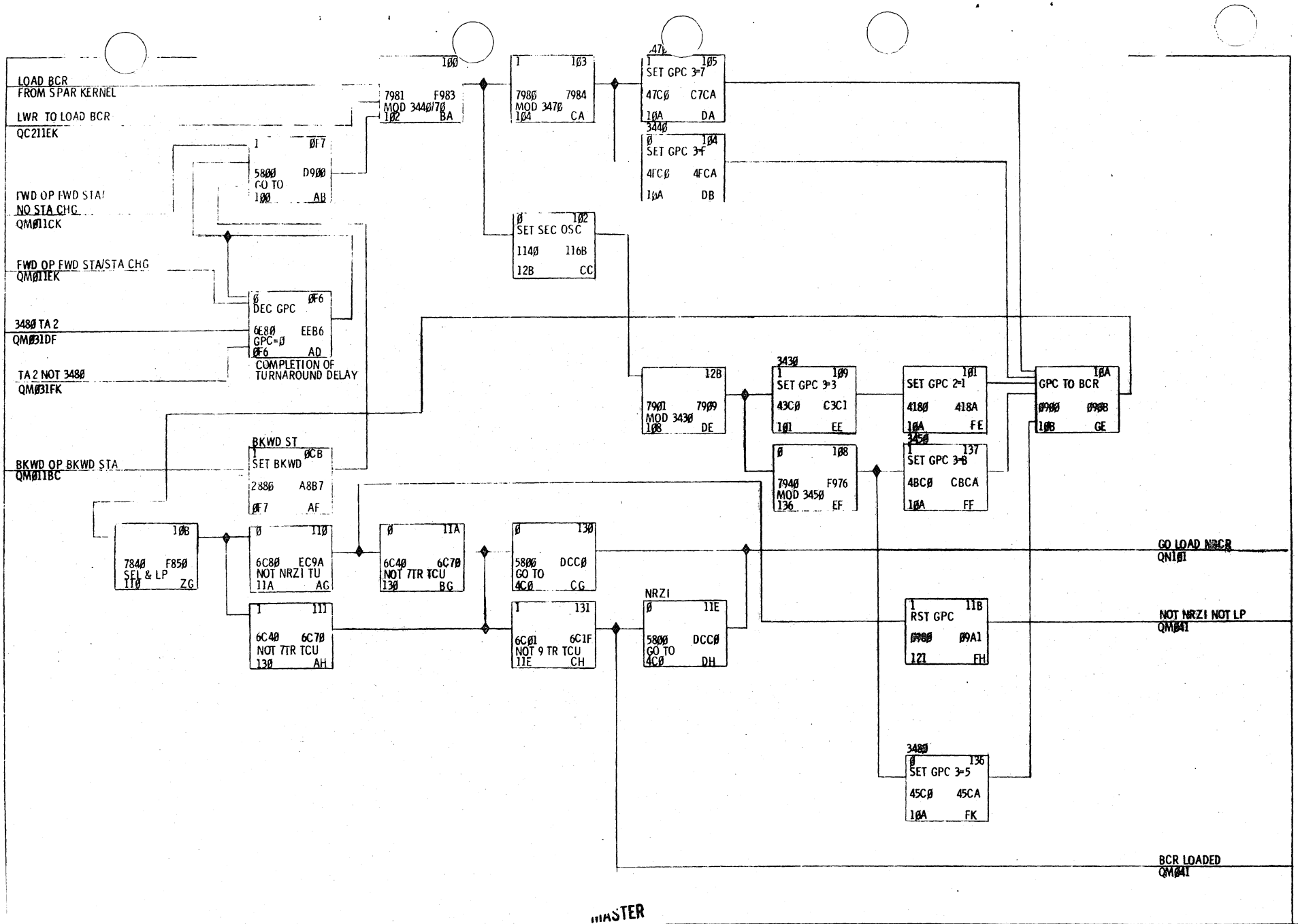
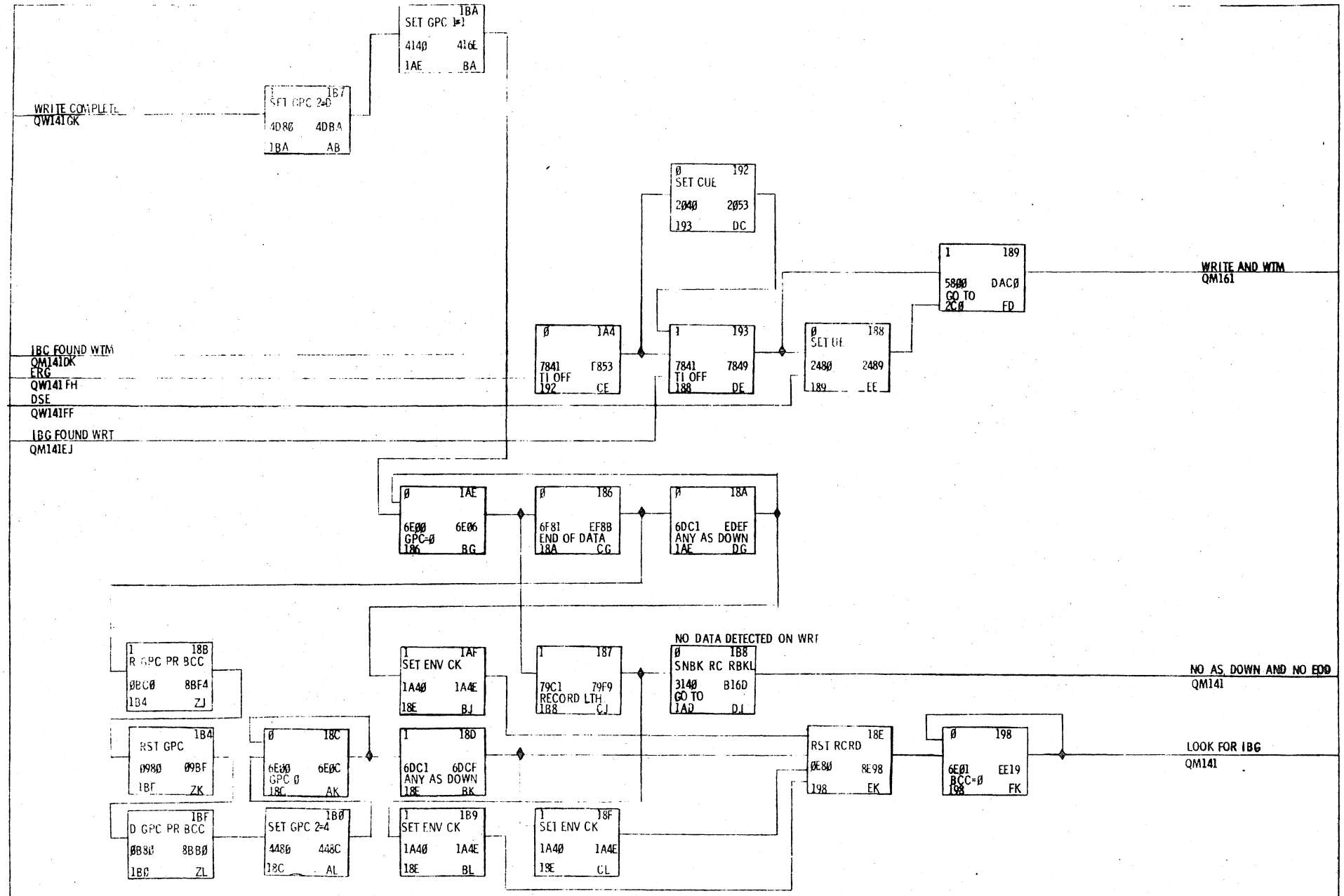
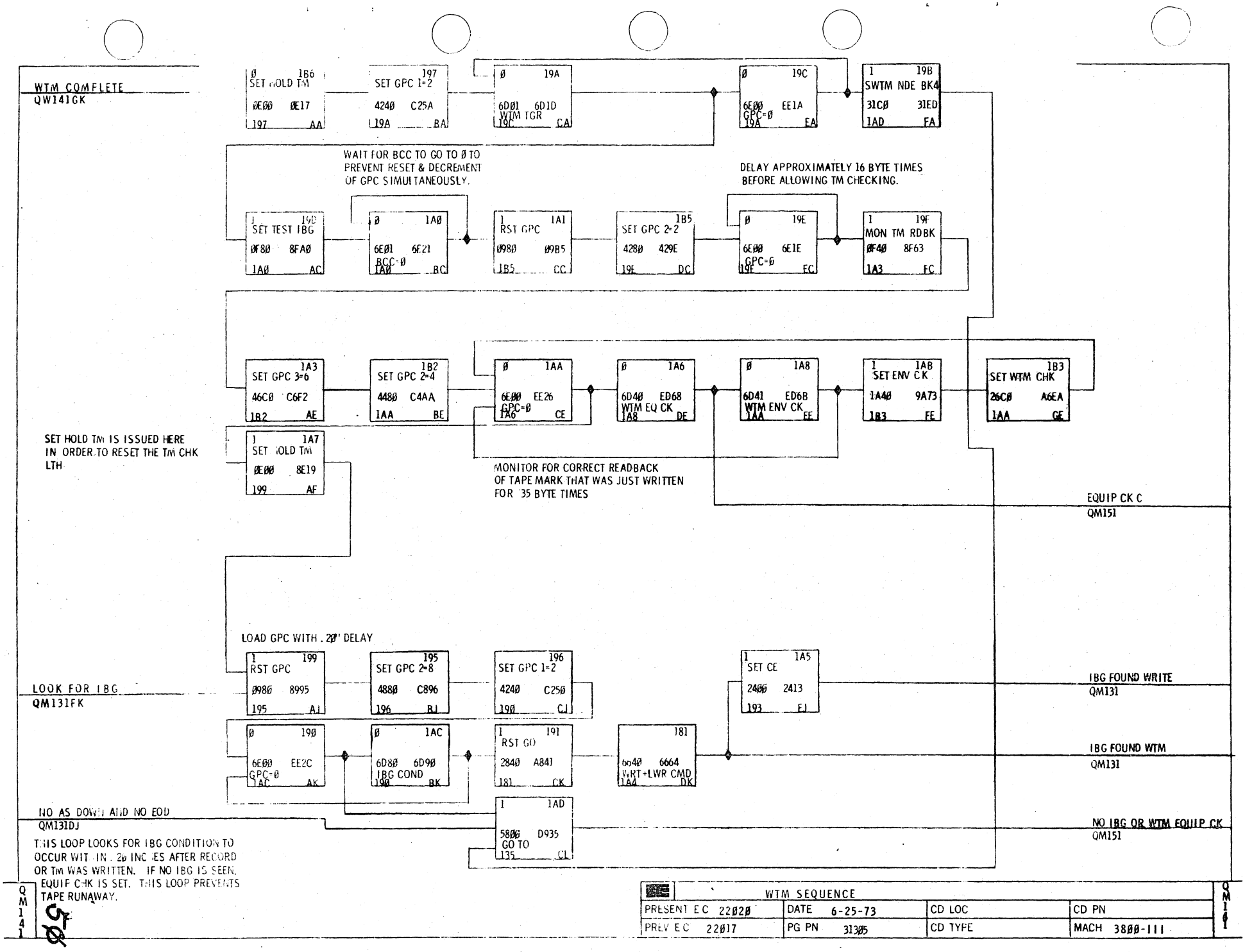

LOAD BCR
FROM SPAR KERNEL
LWR TO LOAD BCR
QC211EK
FWD OP FWD STA/
NO STA CHG
QMØ11CK
FWD OP FWD STA/STA CHG
QMØ11EK
348Ø TA 2
QMØ31DF
TA 2 NOT 348Ø
QMØ31FK
BKWD OP BKWD STA
QMØ11BC
BKWD ST
SET BKWD
COMPLETION OF TURNAROUND DELAY
DEC GPC
GPC=Ø
GO TO
MOD 344Ø/7Ø
MOD 347Ø
MOD 343Ø
MOD 345Ø
SET GPC 3=7
SET GPC 3=F
SET SEC OSC
SET GPC 3=3
SET GPC 2=1
GPC TO BCR
SET GPC 3=B
SEL & LP
NOT NRZI TU
NOT 7TR TCU
NOT 9 TR TCU
NRZI
RST GPC
SET GPC 3=5
GO LOAD NRCB
QN1Ø1
NOT NRZI NOT LP
QMØ41
BCR LOADED
QMØ41
LOAD BCR WITH BIT CELL COUNT
PRESENT E C 22Ø2Ø
PREV E C 22Ø15
DATE 7-9-73
PG PN 3133
CD LOC
CD TYPE
CD PN
MACH 38ØØ-111
QM121



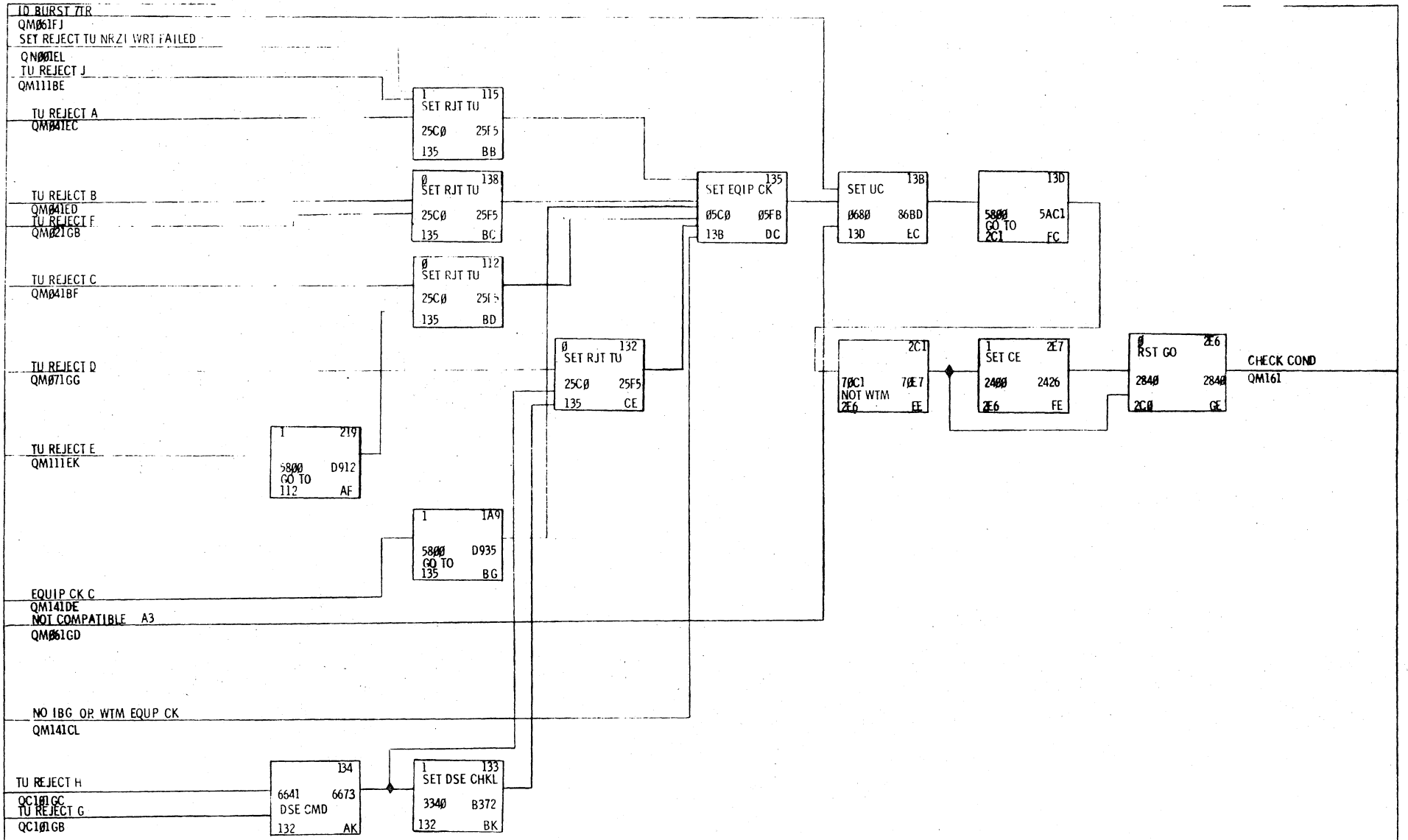
PE WRITE ENDING SEQUENCE				
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22017	PG PN 31304	CD TYPE QM	MACH 3800-111	

QM131 64 QM131



WTM SEQUENCE			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C 22Ø17	PG PN 313Ø5	CD TYPE	MACH 38ØØ-111

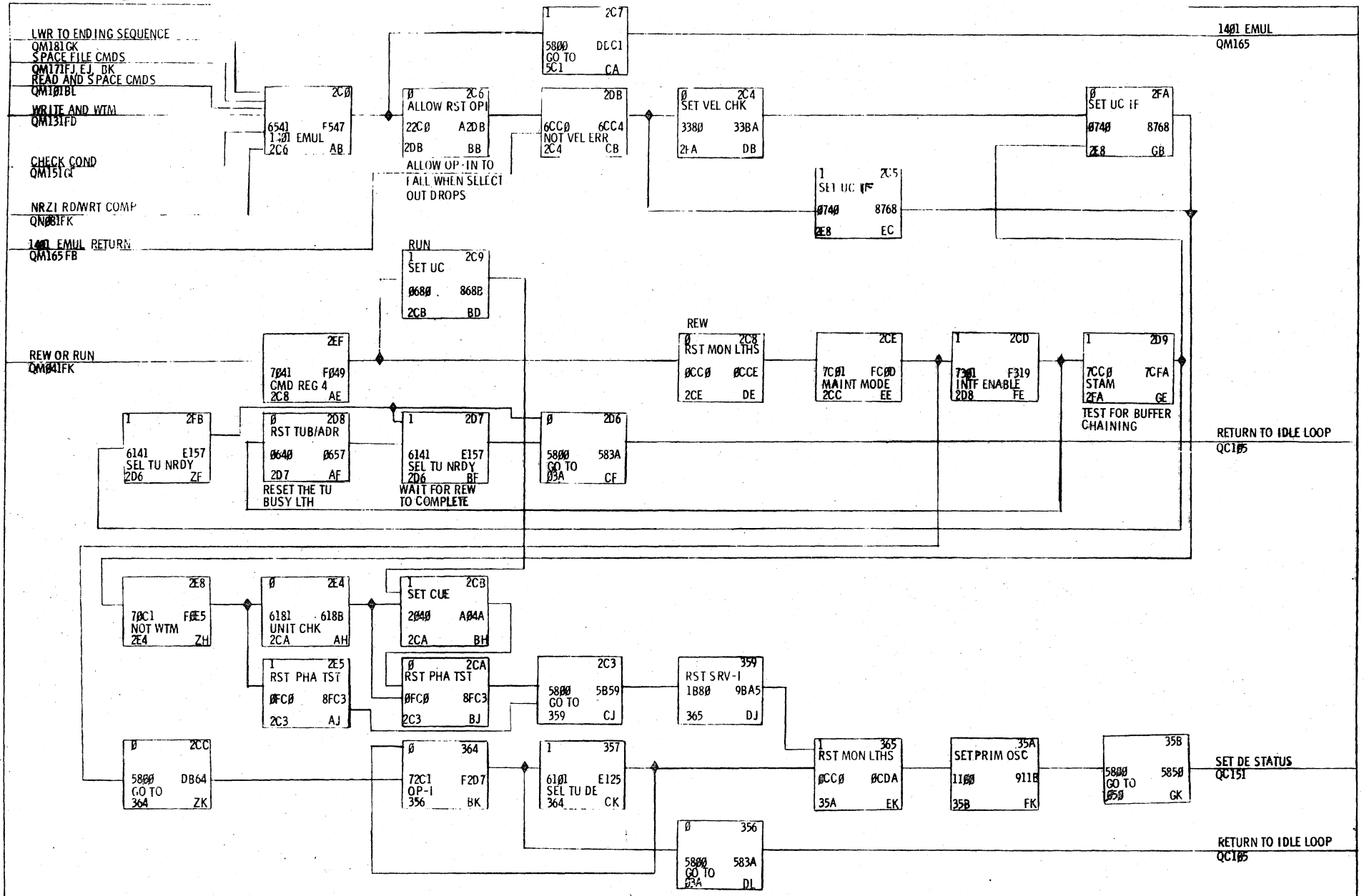
QM141 QM141



MASTER

CHECK CONDITIONS			
PRESENT E.C 22Ø2Ø	DATE 7-9-73	CD LOC	CD PN
PREV E.C 22Ø15	PG PN 31366	CD TYPE	MACH 38ØØ-111

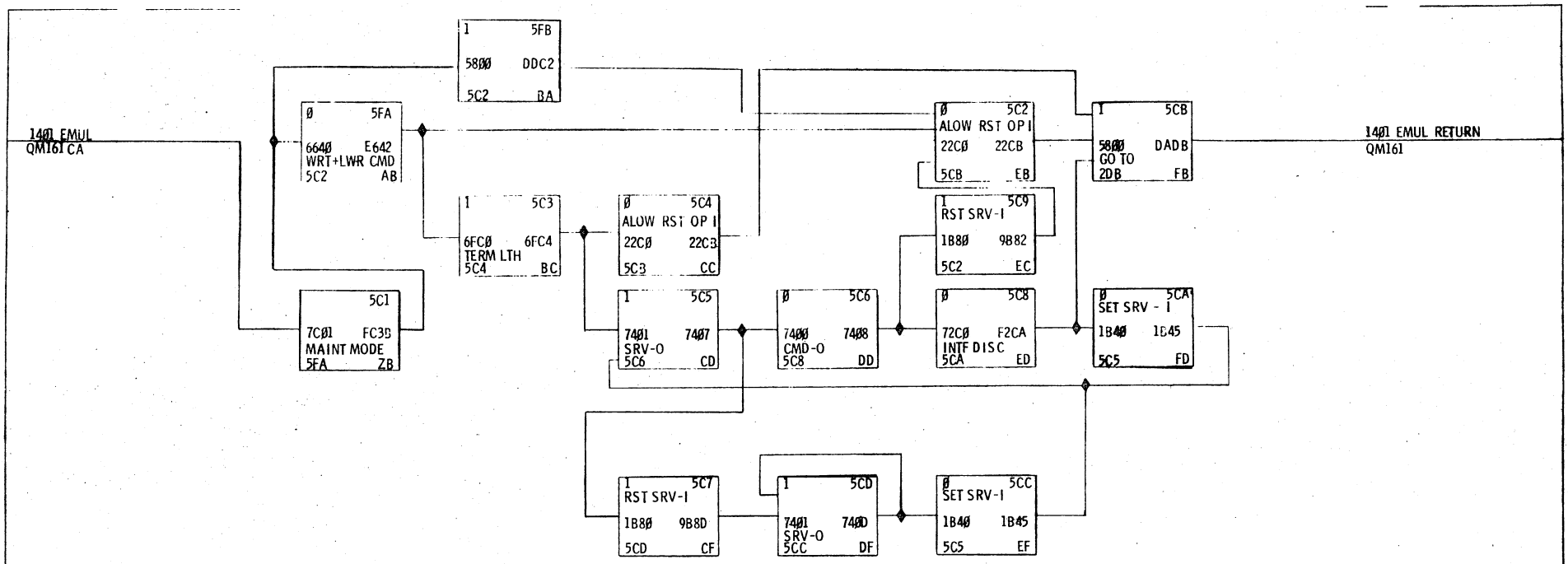
QM151 QM151



MASTER

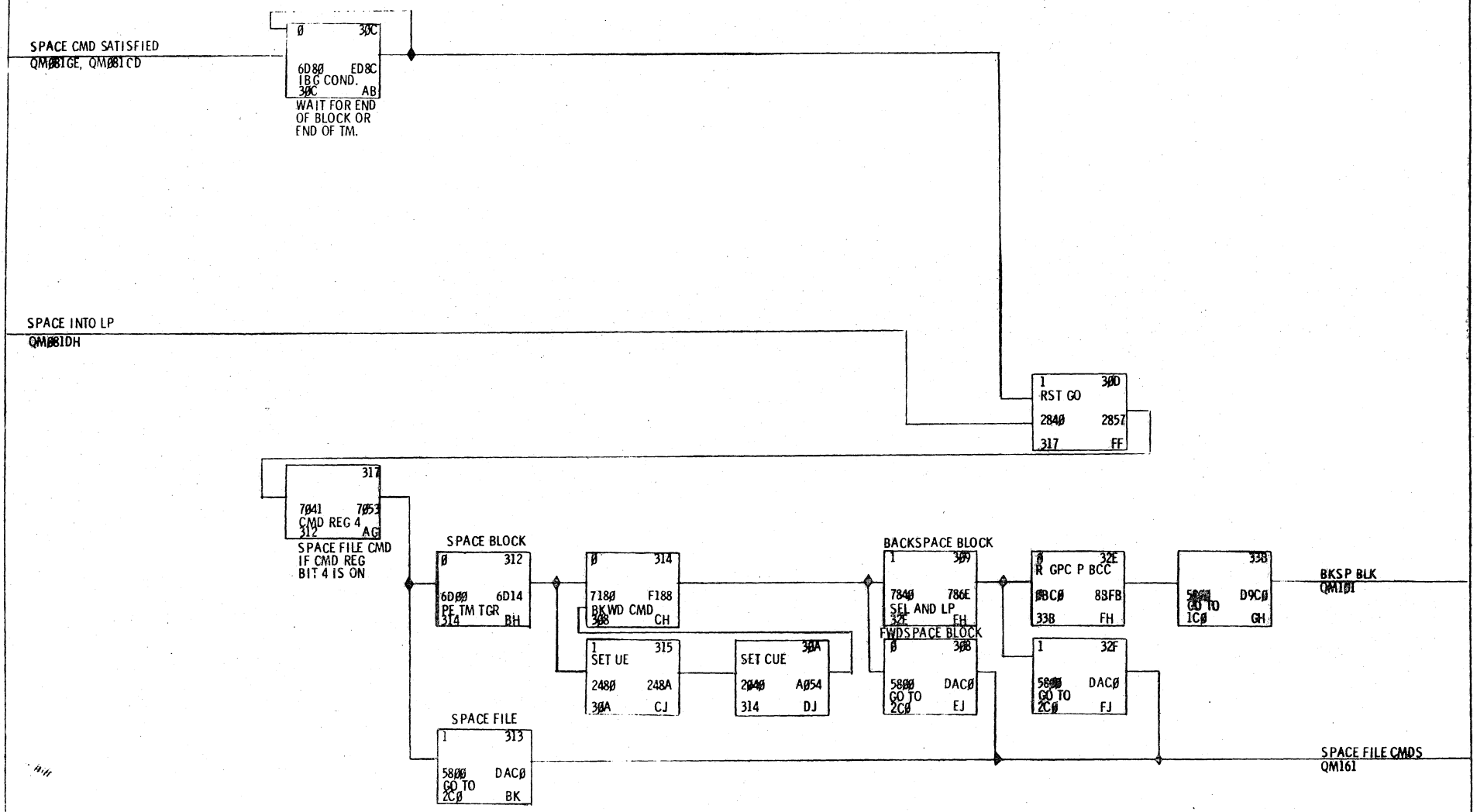
ENDING SEQUENCE			
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN
PREV E C 22015	PG PN 31307	CD TYPE QM	MACH 3800-111

QM161

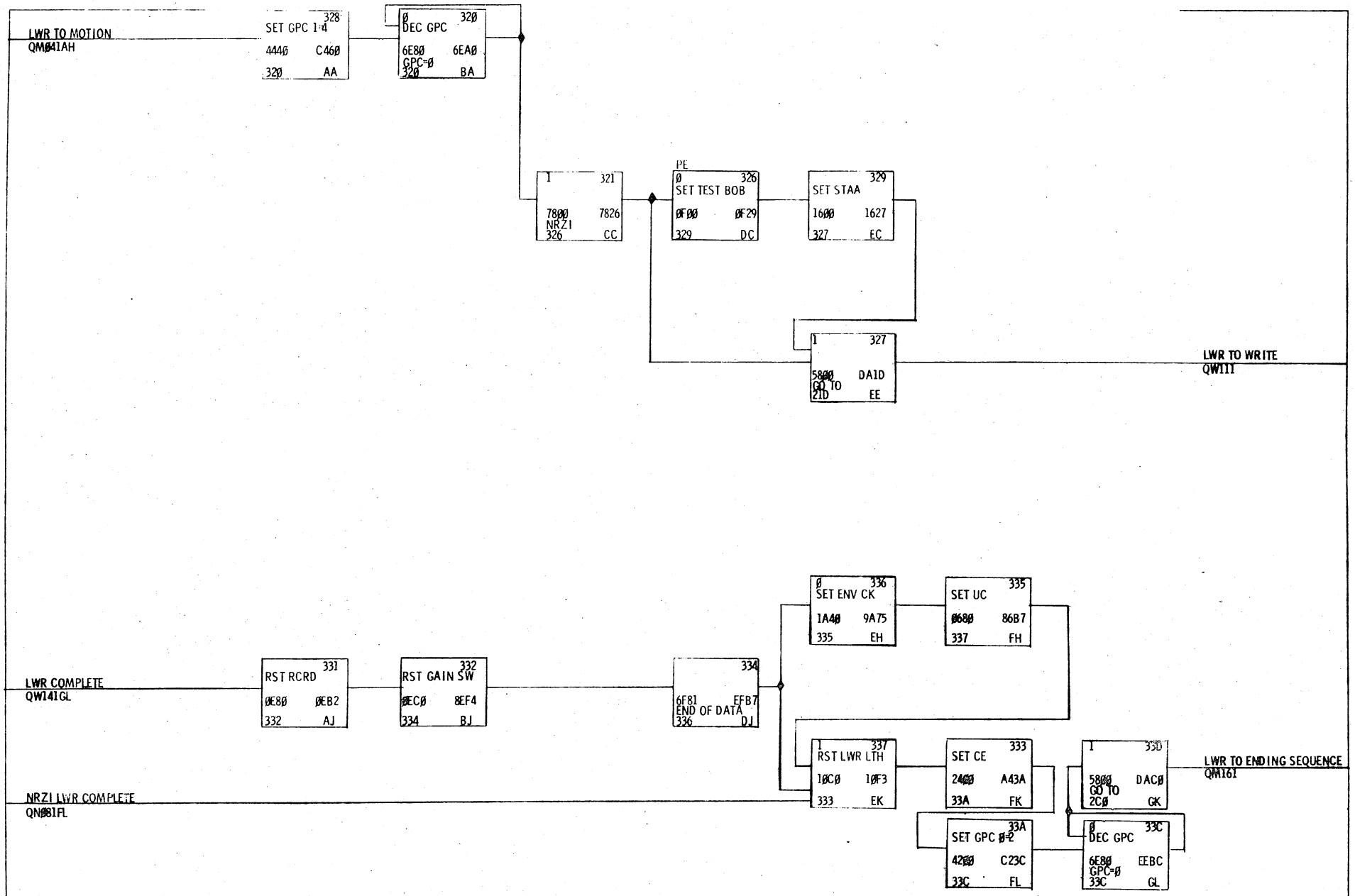


THIS LOOP IS DESIGNED TO COMPLETE THE TRANSMISSION OF A BLOCK OF DATA, EVEN THOUGH THE TERMINATE LATCH MAY HAVE COME ON. THE 1401 EMULATOR REQUIRES THAT THE CONTROL UNIT ACCEPT ALL OF THE DATA. JUMPER NOT REQUIRED ON A STANDALONE.

MOD 30 WITH EMULATION			
PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN
PREV EC 22015	PG PN 31388	CD TYPE QM	MACH



END SPACE CMDS -TEST FOR IBG			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV EC 22Ø15	PG PN 313Ø9	CD TYPE	MACH 38ØØ-111



QM181	LWR ENTRY EXIT ROUTINE				QM181
	PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
	PREV E C 22Ø12	PG PN 3131Ø	CD TYPE	MACH 38ØØ-111	

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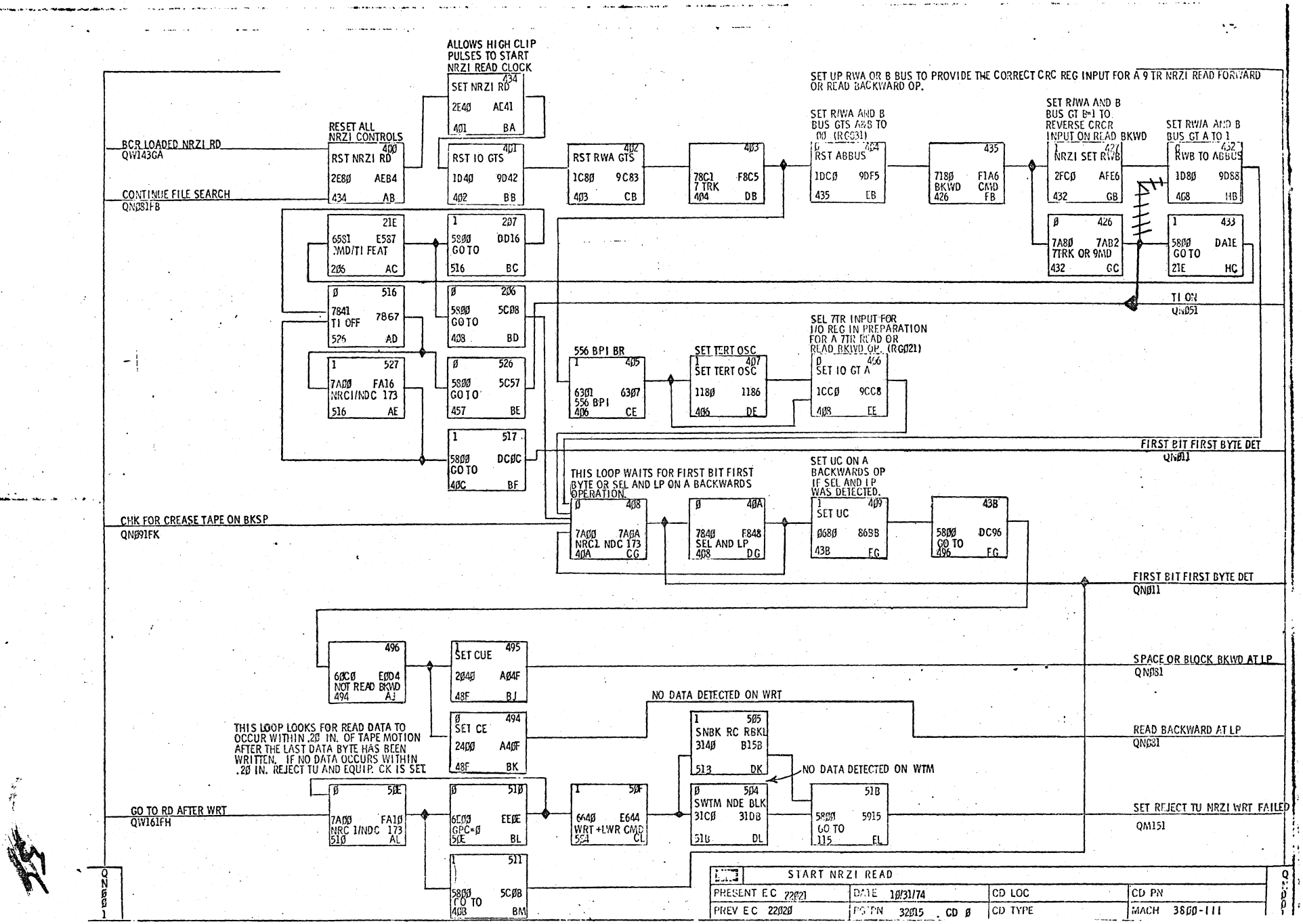
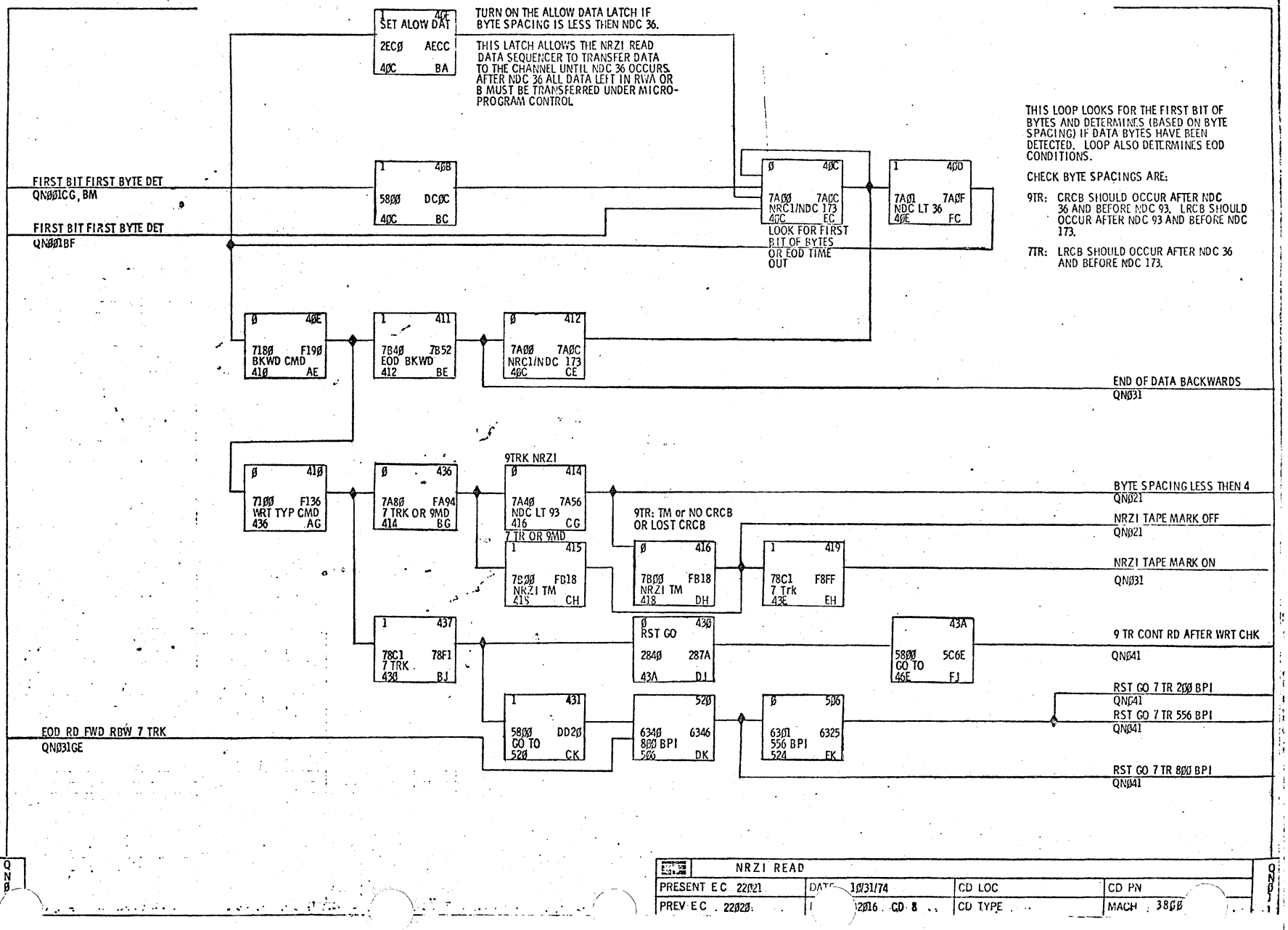
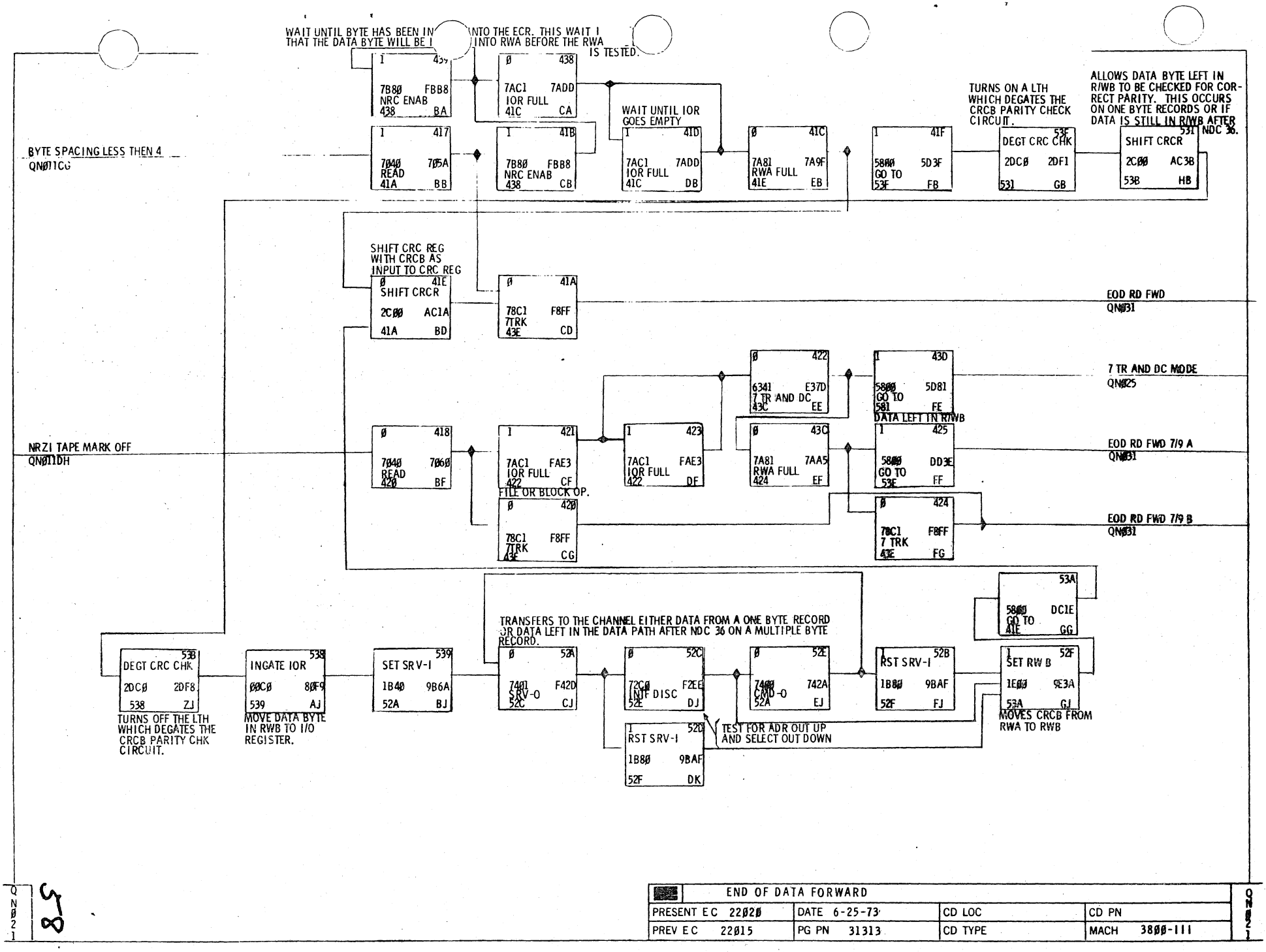
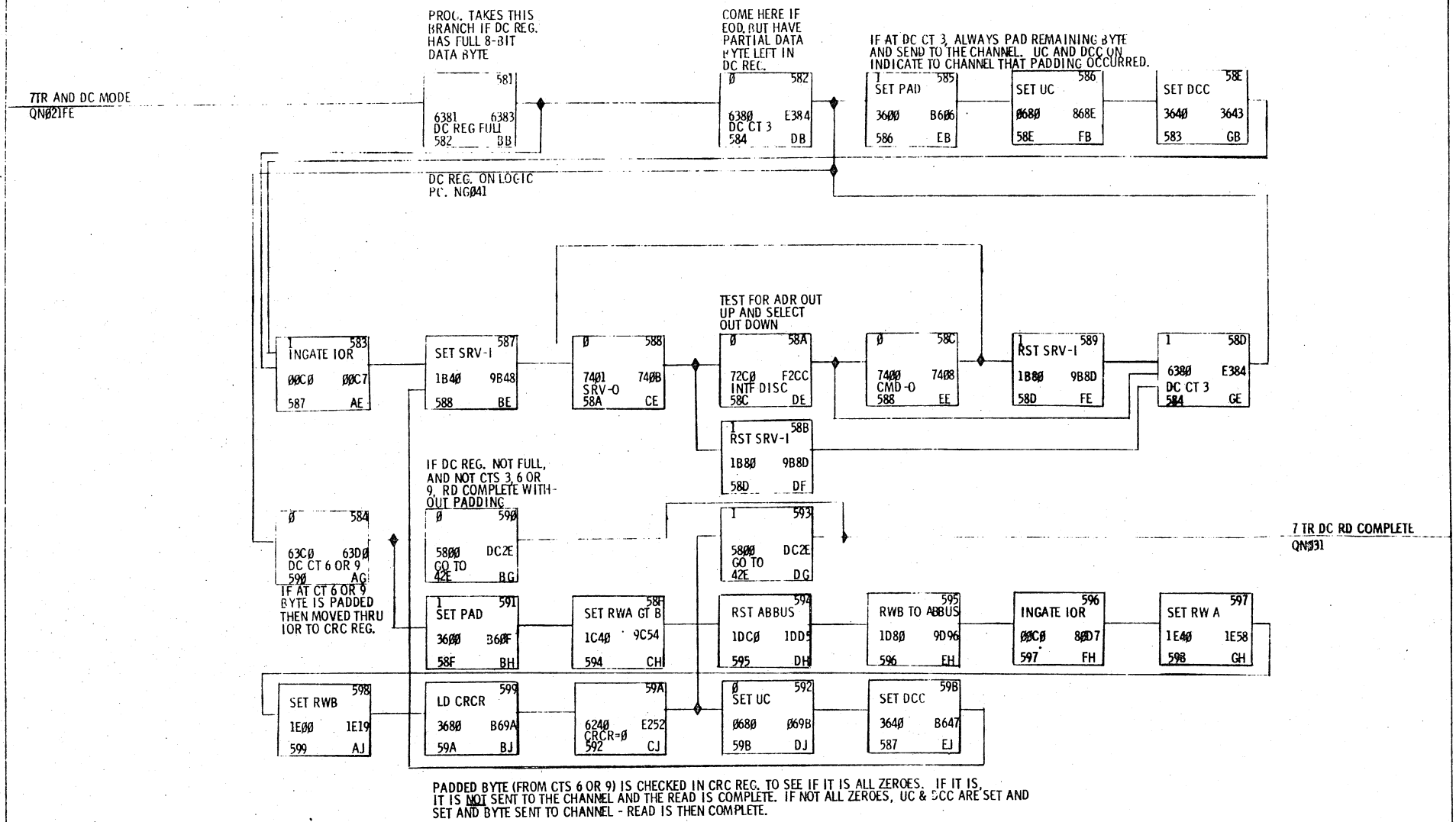

ALLOWS HIGH CLIP PULSES TO START NRZI READ CLOCK
SET NRZI RD 434
SET UP RWA OR B BUS TO PROVIDE THE CORRECT CRC REG INPUT FOR A 9 TR NRZI READ FORWARD OR READ BACKWARD OP.
SET RWA AND B BUS GTS A&B TO 00 (RG031)
SET RWA AND B BUS GT B=1 TO REVERSE CRCR INPUT ON READ BKWD
SET RWA AND B BUS GT A TO 1
RESET ALL NRZI CONTROLS
BCR LOADED NRZI RD
QW143GA
CONTINUE FILE SEARCH
QN081FB
RST NRZI RD 400
RST IO GTS 401
RST RWA GTS 402
403
RST ABBUS 404
435
NRZI SET RWB 427
RWB TO ABBUS 432
21E
7MD/TI FEAT
206
GO TO 207
516
GO TO 433
21E
7TRK OR 9MD 426
432
TI ON
QN051
GO TO 516
GO TO 206
GO TO 527
GO TO 526
GO TO 517
457
GO TO 4ØC
556 BPI BR 405
556 BPI 63Ø1
406
SET TERT OSC 407
SET IO GT A 406
SEL 7TR INPUT FOR I/O REG IN PREPARATION FOR A 7TR READ OR READ BKWD OP. (RGØ21)
FIRST BIT FIRST BYTE DET
QN011
THIS LOOP WAITS FOR FIRST BIT FIRST BYTE OR SEL AND LP ON A BACKWARDS OPERATION.
4Ø8
4ØA
SET UC 4Ø9
SET UC ON A BACKWARDS OP IF SEL AND LP WAS DETECTED.
GO TO 43B
CHK FOR CREASE TAPE ON BKSP
QN091FK
FIRST BIT FIRST BYTE DET
QN011
496
NOT READ BKWD
494
SET CUE 495
SPACE OR BLOCK BKWD AT LP
QN081
NO DATA DETECTED ON WRT
SET CE 494
THIS LOOP LOOKS FOR READ DATA TO OCCUR WITHIN .2Ø IN. OF TAPE MOTION AFTER THE LAST DATA BYTE HAS BEEN WRITTEN. IF NO DATA OCCURS WITHIN .2Ø IN. REJECT TU AND EQUIP. CK IS SET.
SNBK RC RBKL 505
READ BACKWARD AT LP
QN081
NO DATA DETECTED ON WTM
GO TO RD AFTER WRT
QW161FH
GPC=Ø 51Ø
WRT +LWR CMD 5Ø4
SWTM NDE BLK 5Ø4
GO TO 51B
GO TO 5915
SET REJECT TU NRZI WRT FAILED
QM151
GO TO 511
GO TO 5CØB
START NRZI READ
PRESENT E C 22Ø21
DATE 1Ø/31/74
CD LOC
CD PN
PREV E C 22Ø2Ø
PG PN 32Ø15
CD Ø
CD TYPE
MACH 38ØØ-111


1 40F
SET ALOW DAT
2EC0 AECC
40C BA
TURN ON THE ALLOW DATA LATCH IF BYTE SPACING IS LESS THEN NDC 36.
THIS LATCH ALLOWS THE NRZI READ DATA SEQUENCER TO TRANSFER DATA TO THE CHANNEL UNTIL NDC 36 OCCURS. AFTER NDC 36 ALL DATA LEFT IN RWA OR B MUST BE TRANSFERRED UNDER MICRO-PROGRAM CONTROL
THIS LOOP LOOKS FOR THE FIRST BIT OF BYTES AND DETERMINES (BASED ON BYTE SPACING) IF DATA BYTES HAVE BEEN DETECTED. LOOP ALSO DETERMINES EOD CONDITIONS.
CHECK BYTE SPACINGS ARE:
9TR: CRCB SHOULD OCCUR AFTER NDC 36 AND BEFORE NDC 93. LRCB SHOULD OCCUR AFTER NDC 93 AND BEFORE NDC 173.
7TR: LRCB SHOULD OCCUR AFTER NDC 36 AND BEFORE NDC 173.
FIRST BIT FIRST BYTE DET
QN00ICG, BM
FIRST BIT FIRST BYTE DET
QN00IBF
1 40B
58Ø0 DCØC
40C BC
Ø 40C
7AØØ 7AØC
NRC1/NDC 173
40C EC
LOOK FOR FIRST BIT OF BYTES OR EOD TIME OUT
1 40D
7A01 7A0F
NDC LT 36
40E FC
Ø 40E
7180 F190
BKWD CMD
410 AE
1 411
7B40 7B52
EOD BKWD
412 BE
Ø 412
7AØØ 7AØC
NRC1/NDC 173
40C CE
END OF DATA BACKWARDS
QNØ31
Ø 410
7100 F136
WRT TYP CMD
436 AG
Ø 436
7A80 FA94
7 TRK OR 9MD
414 BG
9TRK NRZI
Ø 414
7A40 7A56
NDC LT 93
416 CG
7 TR OR 9MD
1 415
7B00 FB18
NRZI TM
415 CH
9TR: TM or NO CRCB OR LOST CRCB
Ø 416
7B00 FB18
NRZI TM
418 DH
1 419
78C1 F8FF
7 Trk
43E EH
BYTE SPACING LESS THEN 4
QNØ21
NRZI TAPE MARK OFF
QNØ21
NRZI TAPE MARK ON
QNØ31
1 437
78C1 78F1
7 TRK
430 BJ
Ø 430
RST GO
2840 287A
43A DJ
43A
5800 5C6E
GO TO
46E FJ
9 TR CONT RD AFTER WRT CHK
QNØ41
1 431
5800 DD20
GO TO
520 CK
520
6340 6346
800 BPI
506 DK
Ø 506
6301 6325
556 BPI
524 EK
RST GO 7 TR 200 BPI
QNØ41
RST GO 7 TR 556 BPI
QNØ41
RST GO 7 TR 800 BPI
QNØ41
EOD RD FWD RBW 7 TRK
QN031GE
NRZI READ
PRESENT E C 22021
PREV E C 22020
CD LOC
CD PN
CD TYPE
MACH 3800


WAIT UNTIL BYTE HAS BEEN IN
THAT THE DATA BYTE WILL BE I
NTO THE ECR. THIS WAIT I
INTO RWA BEFORE THE RWA
IS TESTED.
7B8Ø FBB8
NRC ENAB
438 BA
7AC1 7ADD
IOR FULL
41C CA
WAIT UNTIL IOR
GOES EMPTY
7AC1 7ADD
IOR FULL
41C DB
7A81 7A9F
RWA FULL
41E EB
TURNS ON A LTH
WHICH DEGATES THE
CRCB PARITY CHECK
CIRCUIT.
DEGT CRC CHK
2DCØ 2DF1
531 GB
ALLOWS DATA BYTE LEFT IN
R/WB TO BE CHECKED FOR COR-
RECT PARITY. THIS OCCURS
ON ONE BYTE RECORDS OR IF
DATA IS STILL IN R/WB AFTER
NDC 36.
SHIFT CRCR
2CØØ AC3B
53B HB
BYTE SPACING LESS THEN 4
QNØ11CG
7ØAØ 7Ø5A
READ
41A BB
7B8Ø FBB8
NRC ENAB
438 CB
SHIFT CRC REG
WITH CRCB AS
INPUT TO CRC REG
SHIFT CRCR
2CØØ AC1A
41A BD
78C1 F8FF
7TRK
43E CD
EOD RD FWD
QNØ31
6341 E37D
7 TR AND DC
43C EE
7 TR AND DC MODE
QNØ25
DATA LEFT IN R/WB
NRZI TAPE MARK OFF
QNØ11DH
7ØAØ 7Ø6Ø
READ
42Ø BF
7AC1 FAE3
IOR FULL
422 CF
FILE OR BLOCK OP.
7AC1 FAE3
IOR FULL
422 DF
7A81 7AA5
RWA FULL
424 EF
EOD RD FWD 7/9 A
QNØ31
EOD RD FWD 7/9 B
QNØ31
78C1 F8FF
7 TRK
43E CG
78C1 F8FF
7 TRK
43E FG
TRANSFERS TO THE CHANNEL EITHER DATA FROM A ONE BYTE RECORD
OR DATA LEFT IN THE DATA PATH AFTER NDC 36 ON A MULTIPLE BYTE
RECORD.
DEGT CRC CHK
2DCØ 2DF8
538 ZJ
TURNS OFF THE LTH
WHICH DEGATES THE
CRCB PARITY CHK
CIRCUIT.
INGATE IOR
ØØCØ 8ØF9
539 AJ
MOVE DATA BYTE
IN RWB TO I/O
REGISTER.
SET SRV-I
1B4Ø 9B6A
52A BJ
7401 F42D
SRV-O
52C CJ
72CØ F2EE
OUT DISC
52E DJ
7400 742A
CMD-O
52A EJ
RST SRV-I
1B8Ø 9BAF
52F FJ
SET RW B
1EØØ 9E3A
53A GJ
MOVES CRCB FROM
RWA TO RWB
RST SRV-I
1B8Ø 9BAF
52F DK
TEST FOR ADR OUT UP
AND SELECT OUT DOWN
END OF DATA FORWARD
PRESENT E C 22Ø2Ø
DATE 6-25-73
CD LOC
CD PN
PREV E C 22Ø15
PG PN 31313
CD TYPE
MACH 38ØØ-111
QNØ21
QNØ21
58



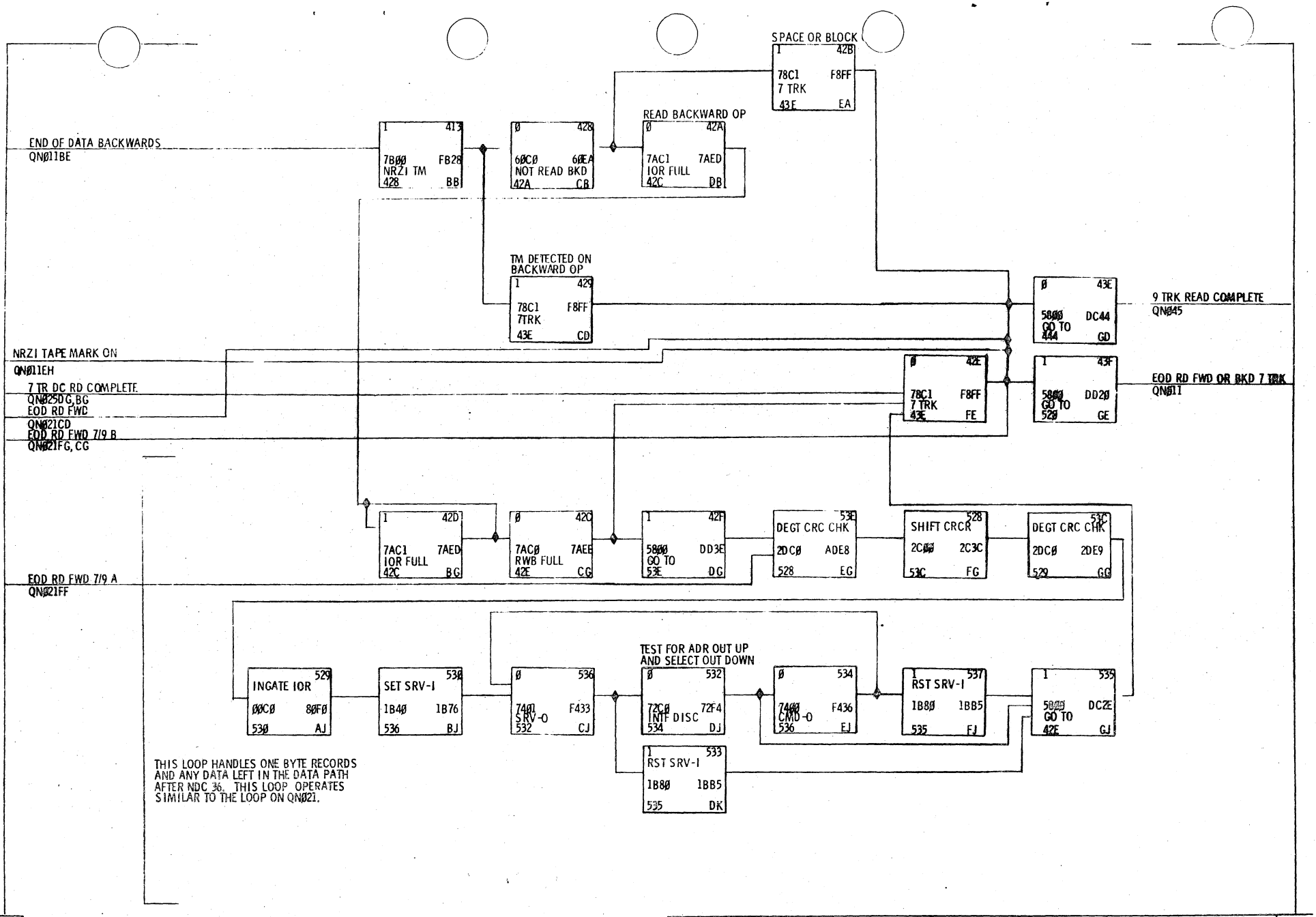
THE PROGRAM ON THIS PAGE IS USED ANY TIME THE TCU IS IN 7 TRK AND DATA CONVERT MODE: IT DETERMINES WHETHER "PADDING" WITH ZEROES WILL OCCUR AT THE END OF A RECORD AND IF THIS "PADDED" BYTE WILL BE SENT TO THE CHANNEL.

REFER TO MOD III FE MANUAL (P. 1-8) FOR DC CT. INFORMATION.

QNØ25 59

DATA CONVERT PADDING- 7 TR			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV EC 22Ø15	PG PN 31314	CD TYPE	MACH 38ØØ-III

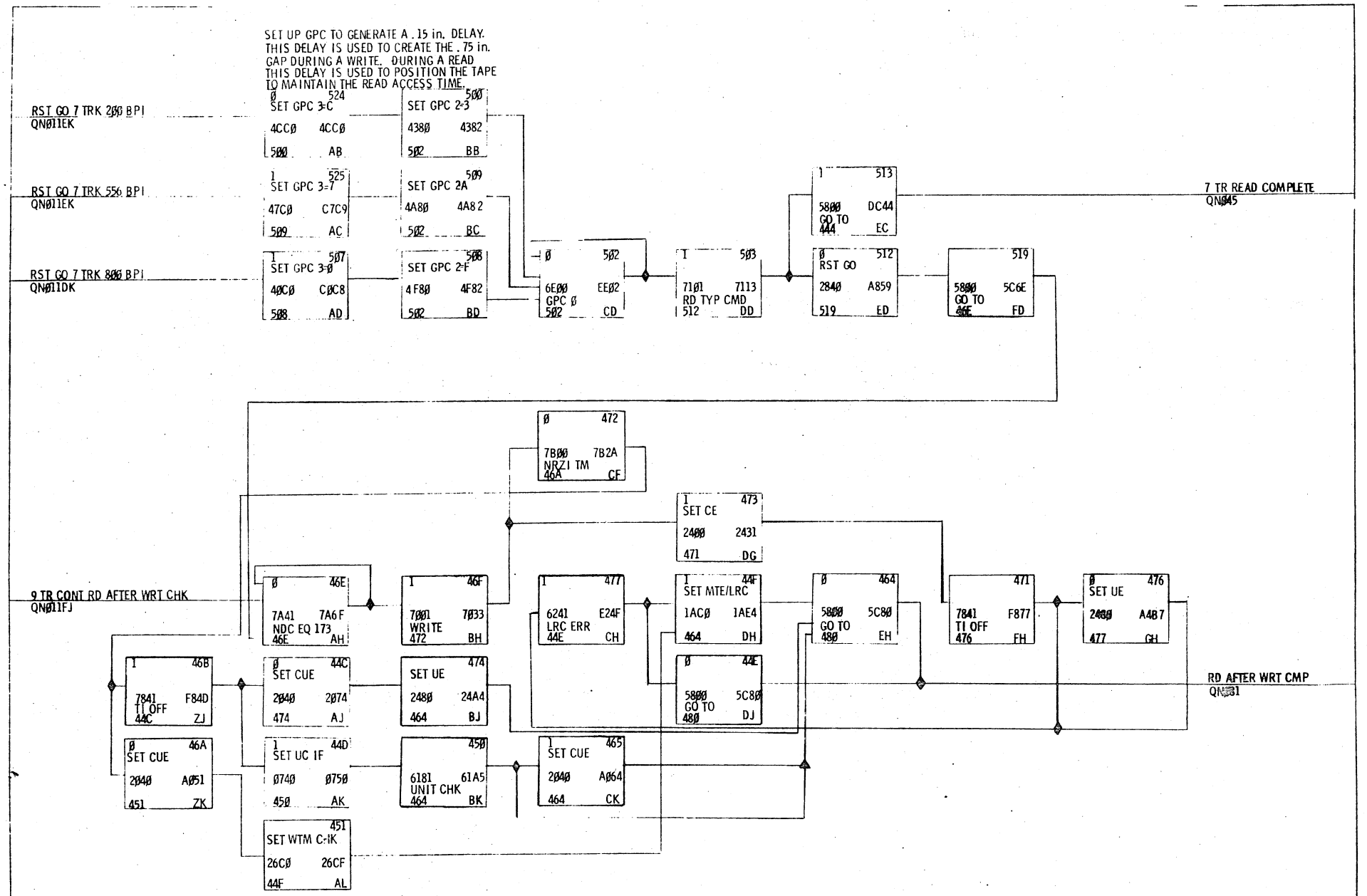
QNØ25



END OF DATA FWD OR BKD				
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22Ø15	PG PN 31315	CD TYPE	MACH 38ØØ-111	

QNØ31

QNØ31



GENERATE NRZI READ STOP DELAY			
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN
PREV E C 22015	PG PN 31316	CD TYPE QN	MACH 3800-111

7 TRK READ COMPLETE
QN041EC
9 TRK READ COMPLETE
QN031GD

Ø 4

7A41 FA45
NDC EQ 173
444 BA

THIS WAIT FOR NDC 173 IS USED TO INSURE THAT ALL CHECK CHARACTERS HAVE BEEN READ BEFORE THE LRC AND CRC REGISTERS ARE CHECKED.

1 445
7Ø4Ø 7Ø48
READ
448 CJ

Ø 448
6ØCØ EØCA
NOT RD BKWD
44A DJ

1 448
58ØØ 5C86
GO TO
486 EJ

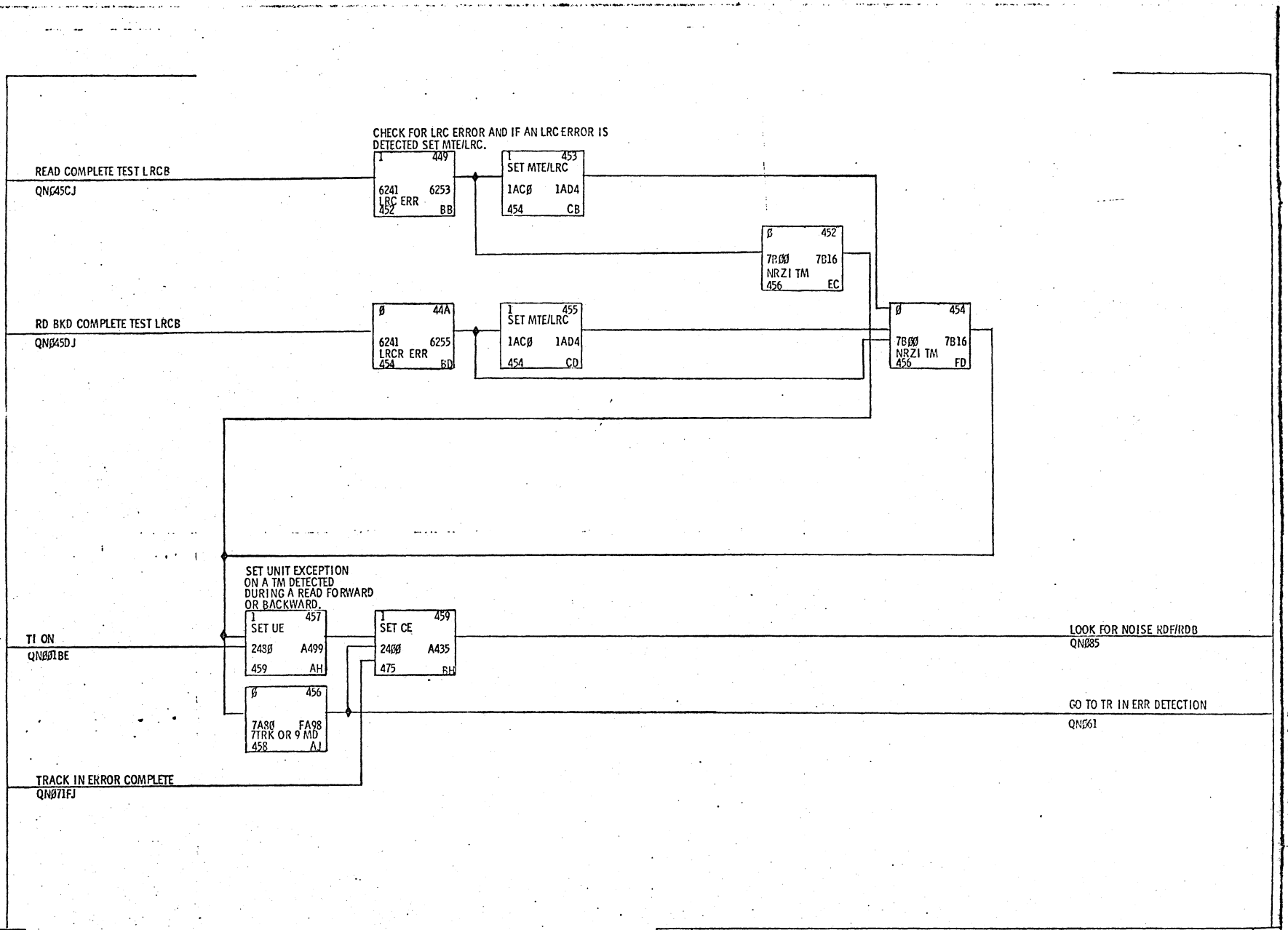
BLOCK OR FILE COMMAND
QN081

RD BKWD COMPLETE TEST LRCB
QN051

READ COMPLETE TEST LRCB
QN051

NRZI STOP DELAY				
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22Ø15	PG PN 31317	CD TYPE	MACH 38ØØ-111	

QN045 62 QN045



LRCB TEST			
PRESENT E C 22Ø21	DAT 1Ø/31/74	CD LOC	CD PN
PREV E C 2202Ø	32Ø17 CD 6	CD TYPE	MACH 38ØØ

USED ONLY FOR 9TR NRZI 800 BPI READ FORWARD/READ BACKWARD OPERATIONS.

GO TO TR IN ERR DETECTION
QN051AJ

SET CRC REG INPUTS TO ZERO SO THAT THE CRC REG CAN BE SHIFTED WITHOUT INPUTS.

458		
RST RWA GTS		
1C80	9CAD	
46D	AB	

46D		
RST AB BUS		
1DC0	9DF0	
470	BB	

470		
NRZI SET RWB		
2FC0	AFFD	
47D	CB	

CHECK FOR MATCH PATTERN (111010111) IN CRC REG.

47D		
6200	E21A	
CRC EQ MATCH		
45A	EB	

CRCR OK
QN071

THIS MICRO PROGRAM ROUTINE CHECKS THE CRCR AFTER EACH READ FOR THE MATCH PATTERN (111010111). THE MATCH PATTERN INSURES THAT THE RECORD WAS READ WITHOUT ERRORS OR IF DOING A CORRECTIVE READ, CORRECTION WAS SUCCESSFUL. IF THE MATCH PATTERN IS NOT FOUND THEN THE CRCR IS CHECKED FIRST FOR ZERO AND IF IT CONTAINS ZERO NO ATTEMPT IS MADE TO FIND THE ERROR. IF THE CRCR DOES NOT EQUAL ZERO OR THE MATCH PATTERN AN ATTEMPT IS MADE TO FIND THE TRACK IN ERROR (TIE). AS LONG AS THE ERROR EXISTS ONLY IN ONE TRACK THE ERROR TRACK CAN BE FOUND.

45A		
6240	625C	
CRCR Ø		
45C	AD	

MOVE ERR PATTERN FROM EPR TO DTR

45C		
EPR TO DJ RG		
15C0	15DE	
45E	BD	

RST EPR AND TURN ON EPR BIT P. THIS BIT IS USED TO KEEP TRACK OF WHICH TRACK IS BEING TESTED FOR TIE.

45E		
RST EPR		
2CC0	ACDF	
45F	CD	

45F		
SET EPR P		
2C40	2C60	
460	DD	

ALLOWS CRCR AND DTR TO BE COMPARED USING ECR BUS.

460		
CRC DTR GATE		
2D80	AD21	
461	ED	

IF DTR EQUALS CRCR THEN TIE HAS BEEN FOUND.

461		
6201	E223	
DTR EQ CRCR		
462	AG	

TRACK IN ERROR FOUND.
IF RD FORWARD THE EPR HAS THE TIE BYTE REVERSED:
EPR-P01234567
TIE-7654321ØP
IF RD BKWD EPR CONTAINS TIE BYTE.

463		
SET FOUND TR		
2F80	2F27	
467	BG	

TIE FOUND RD FWD/BKWD
QN071

ALL TRACKS TESTED AND NO TIE FOUND.

CHECK TO SEE IF EPR BIT 7 IS ON. IF ON, ALL TRACKS HAVE BEEN TESTED AND NOT ABLE TO FIND TIE. IF EPR BIT 7 IS NOT ON, SHIFT CRCR. (THIS SHIFT ALSO ADVANCES THE BIT IN THE EPR TO THE NEXT POSITION).

462		
6280	62A6	
EPR BIT 7 ON		
466	BJ	

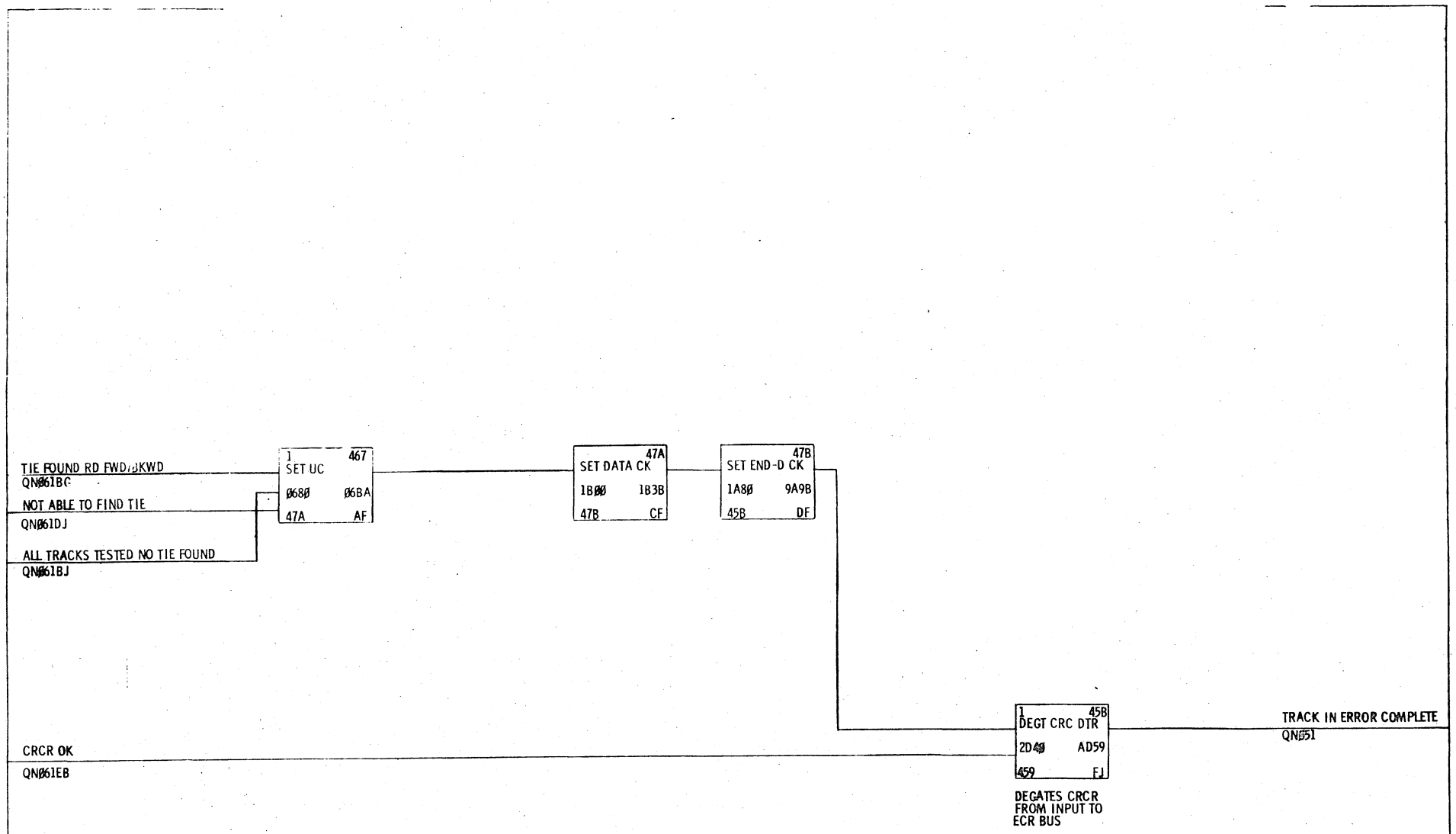
45D		
RST EPR		
2CC0	2CE7	
467	DJ	

NOT ABLE TO FIND TIE
QN071

466		
SHIFT CRCR		
2C80	2C21	
461	CK	

ALL TRACKS TESTED NO TIE FOUND
QN071

CHECK CRCB AND TEST FOR TRACK IN ERROR			
PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN
PREV EC 22015	PG PN 31319	CD TYPE	MACH 3800 - 111

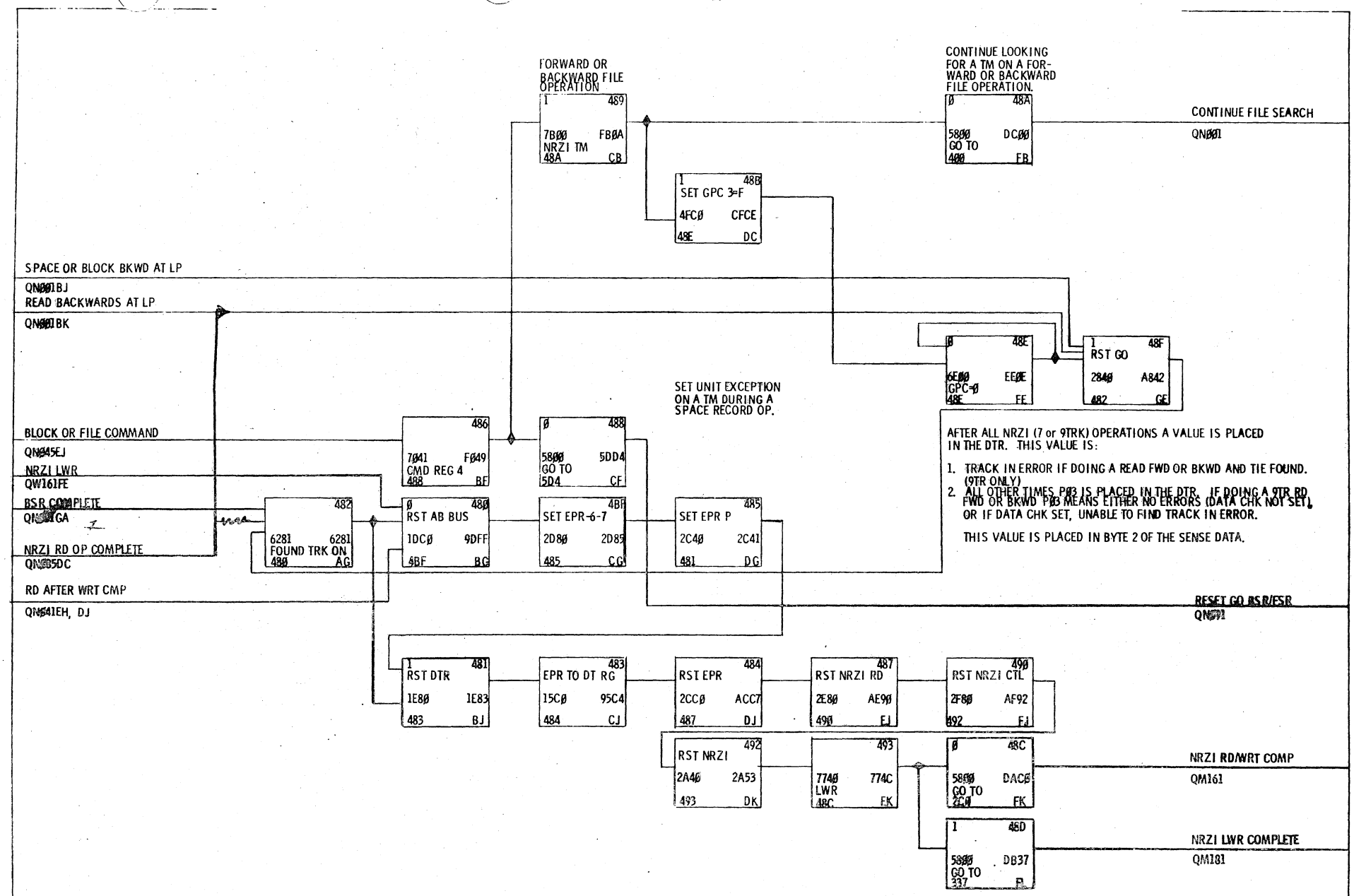


QN061

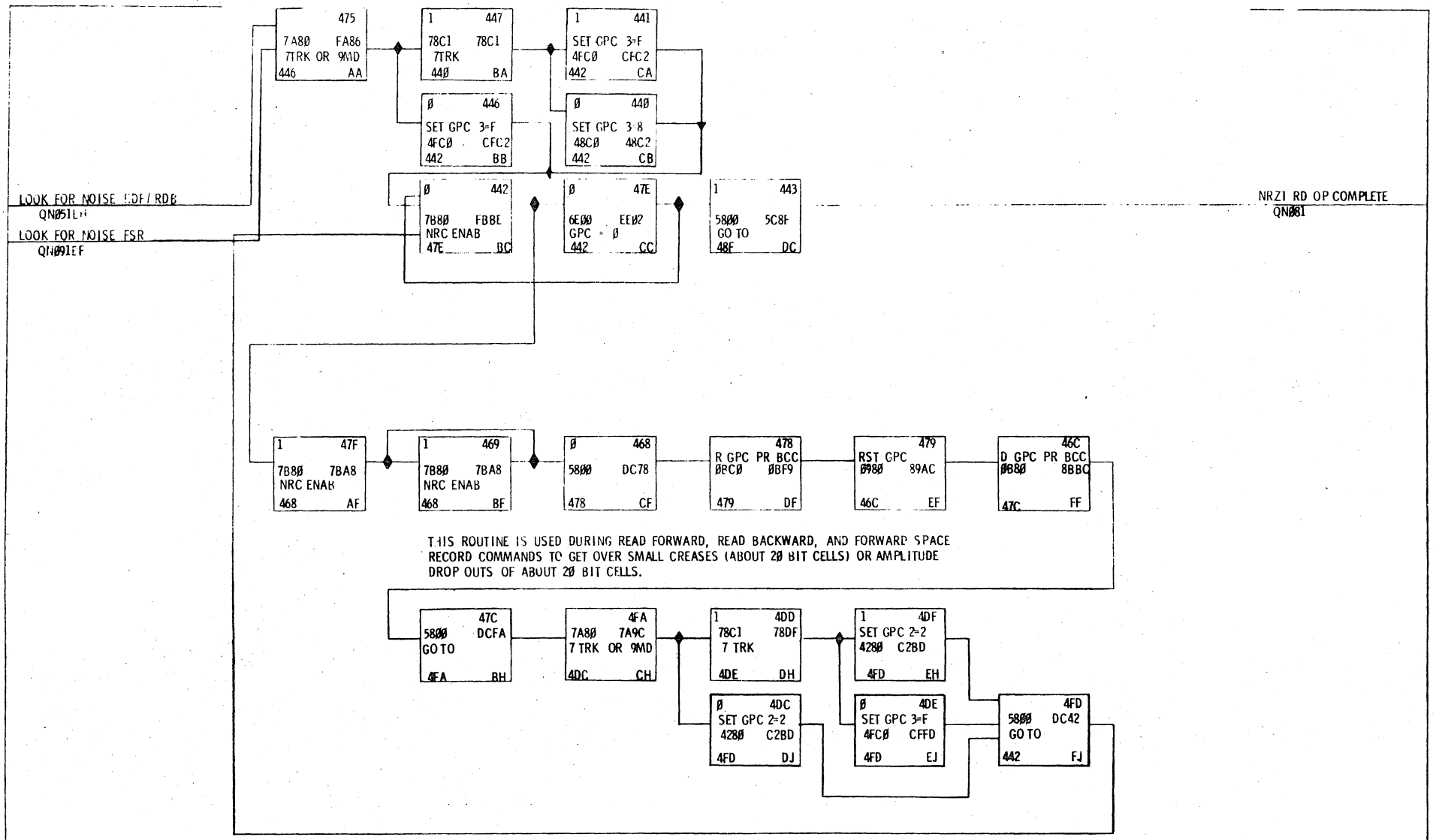
SET DTR WITH TIE DATA

PRESENT EC 22020	DATE 6-25-73	CD LOC	CD PN
PREV EC 22015	PG PN 31320	CD TYPE	MACH 3800 - 111

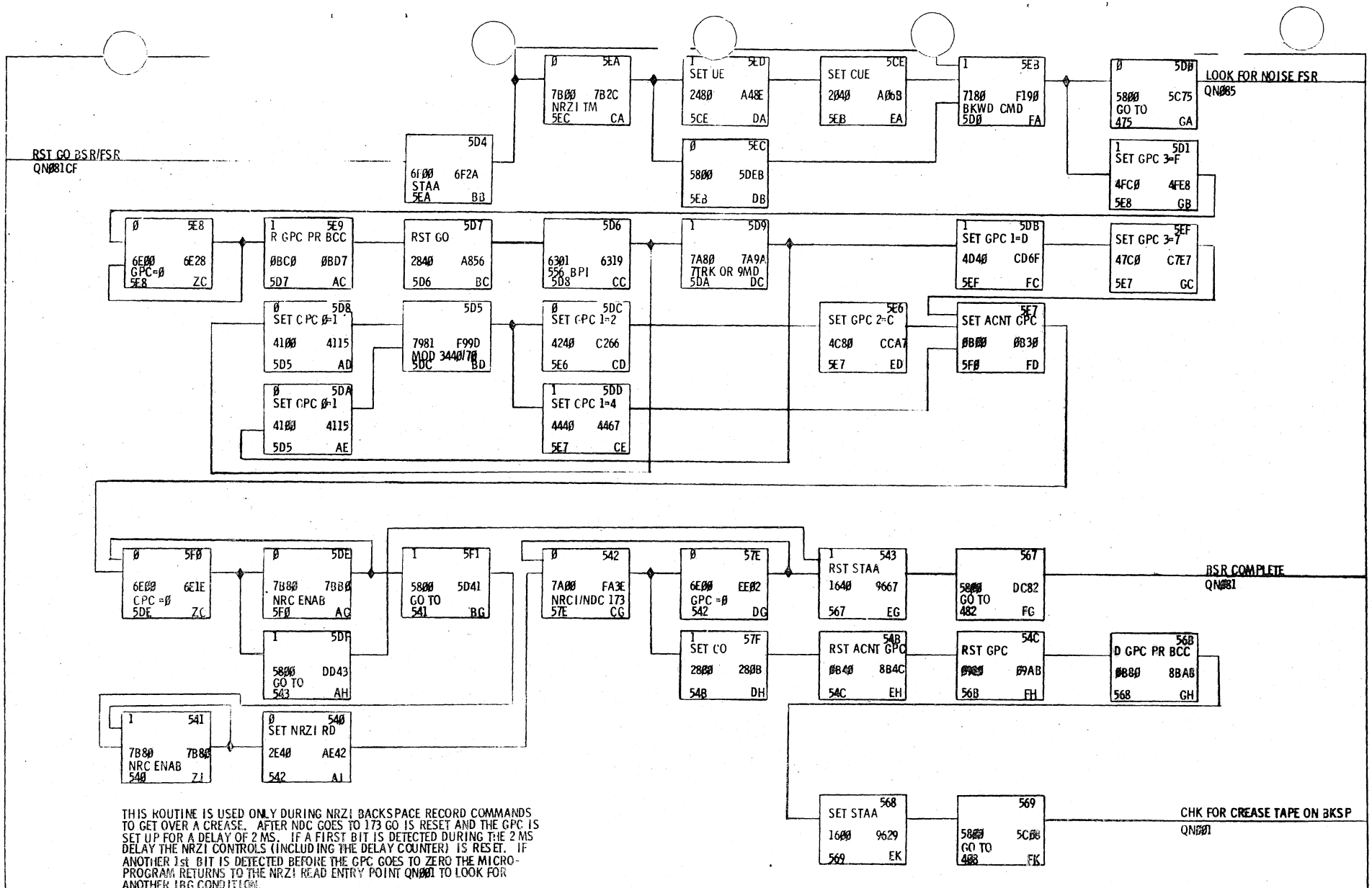
QN061



CHECK FOR STOP DELAY AND NO TM ON FILE CMD			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV EC 22Ø15	PG PN 31321	CD TYPE	MACH 38ØØ - III

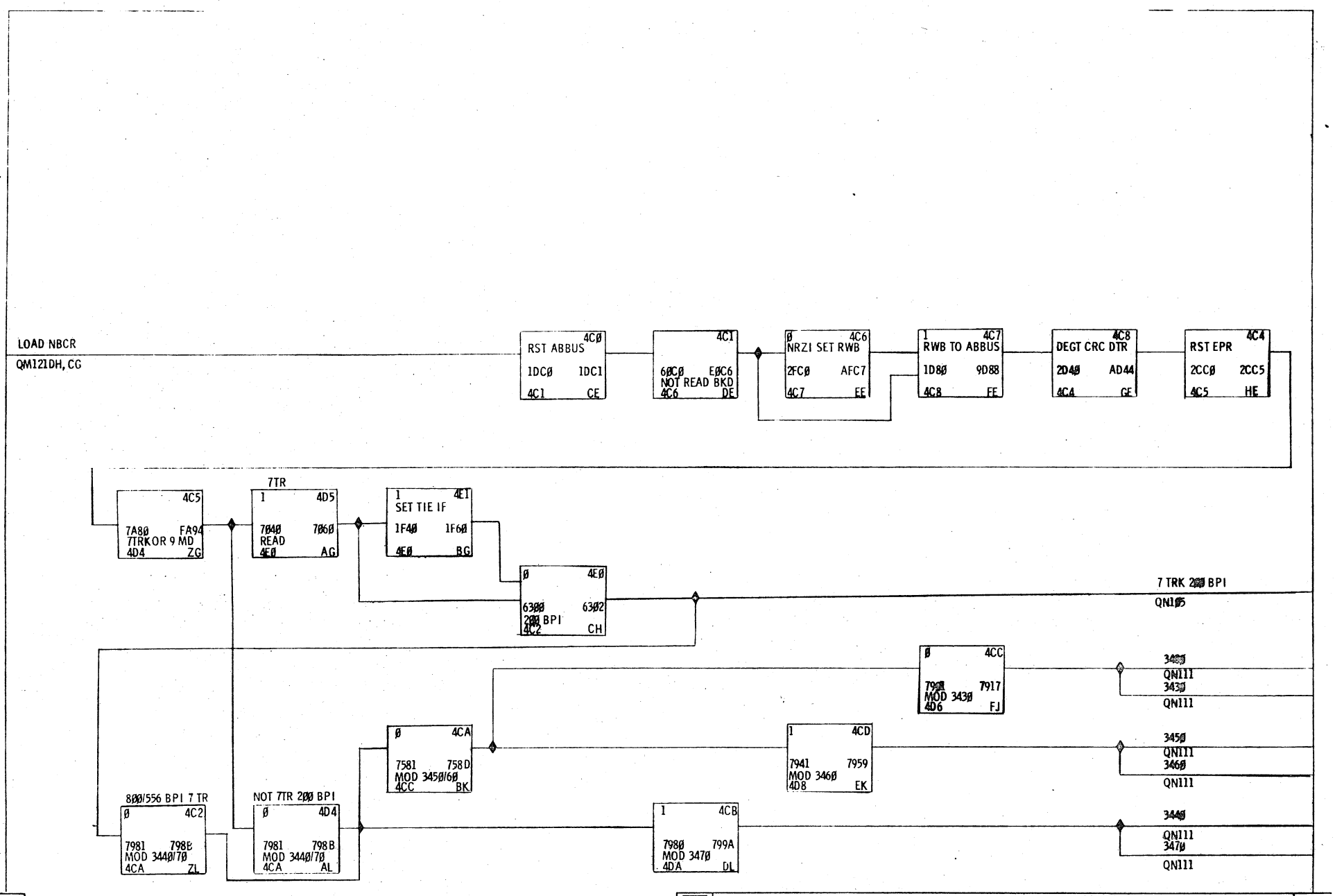


CHK FOR CREASE / VOID - RDF, RDB, OR FSR			
PRESENT E.C 22Ø2Ø	DATE 7-9-73	CD LOC	CD PN
PREV E.C	PG PN 31322	CD TYPE	MACH



THIS ROUTINE IS USED ONLY DURING NRZI BACKSPACE RECORD COMMANDS TO GET OVER A CREASE. AFTER NDC GOES TO 173 GO IS RESET AND THE GPC IS SET UP FOR A DELAY OF 2 MS. IF A FIRST BIT IS DETECTED DURING THE 2 MS DELAY THE NRZI CONTROLS (INCLUDING THE DELAY COUNTER) IS RESET. IF ANOTHER 1st BIT IS DETECTED BEFORE THE GPC GOES TO ZERO THE MICRO-PROGRAM RETURNS TO THE NRZI READ ENTRY POINT QNØØ1 TO LOOK FOR ANOTHER IBG CONDITION.

NRZI CREASE TAPE DELAY				
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
PREV EC 22Ø18	PG PN 31323	CD TYPE	MACH 38ØØ-111	

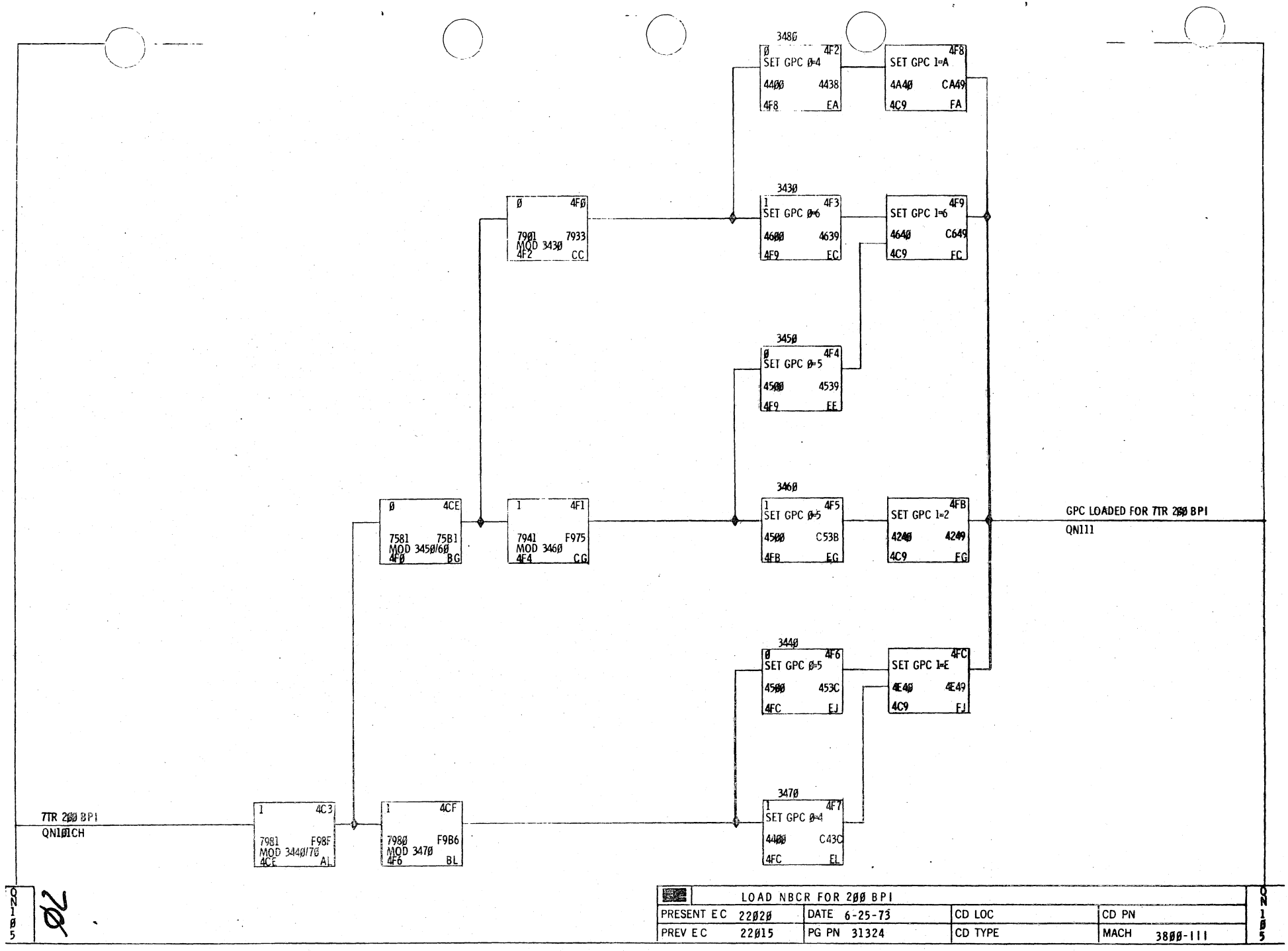


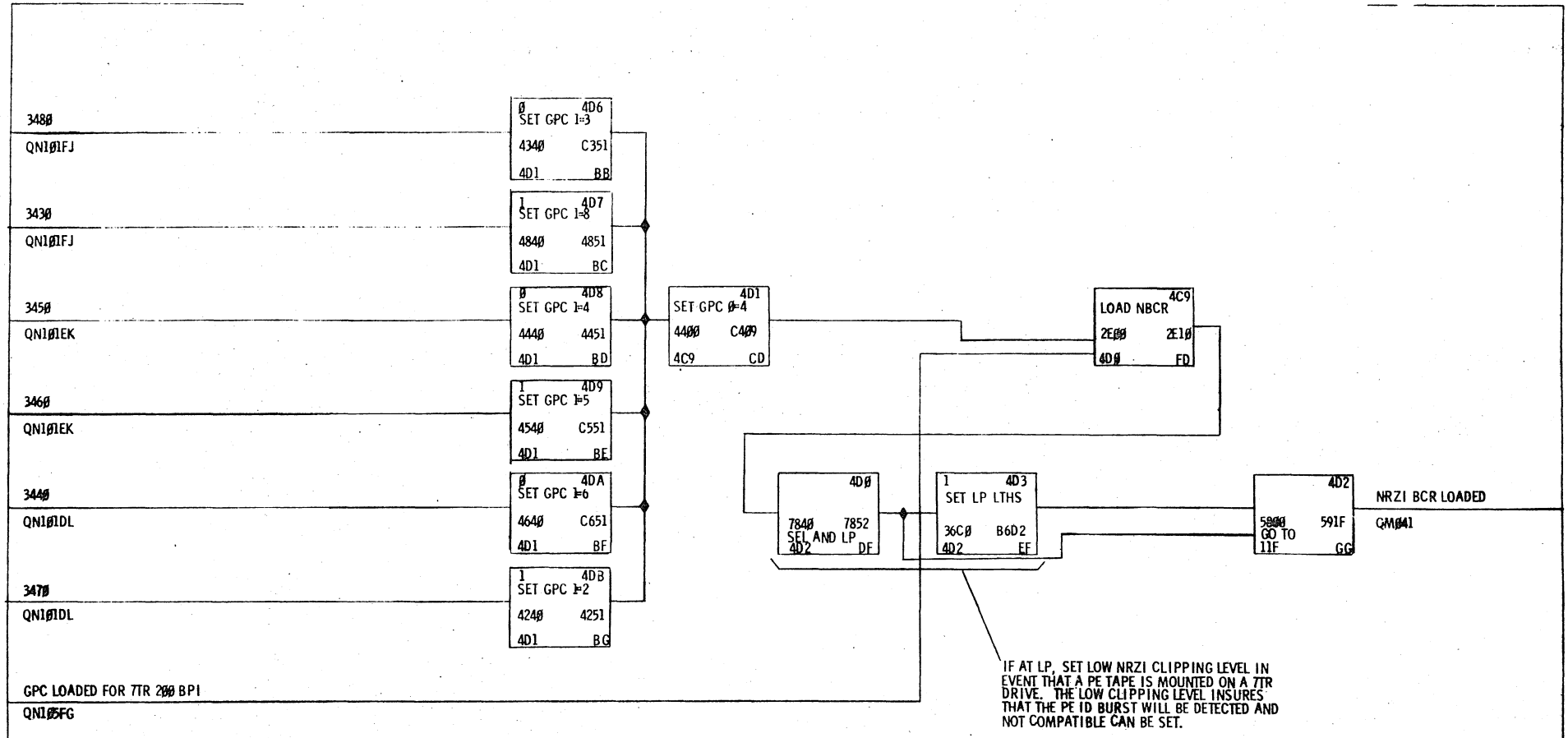
LOAD GPC NBCR AND SKEW GATE VALUES			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV EC 22Ø13	PG PN 31382	CD TYPE	MACH 38ØØ

QN181

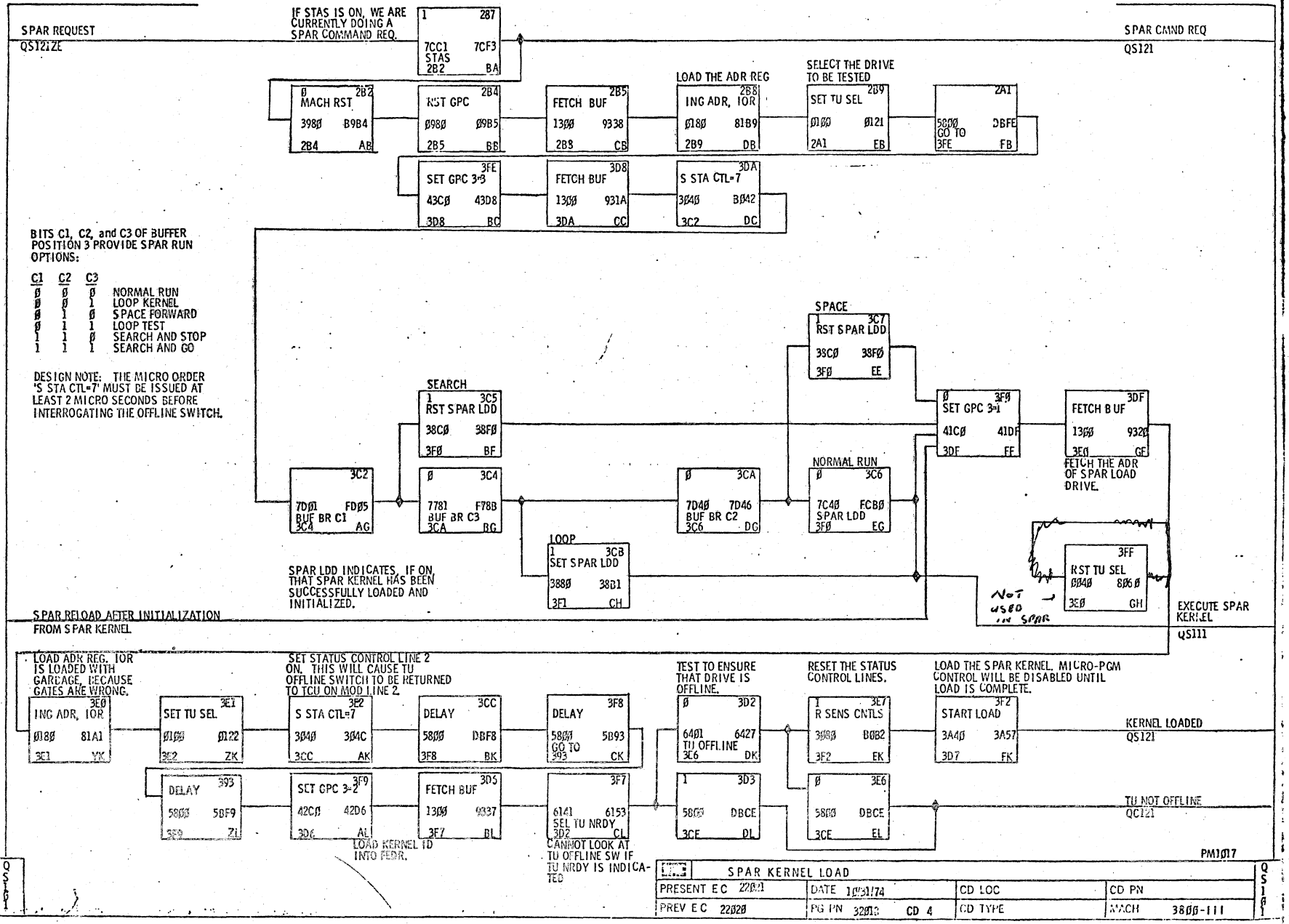
69

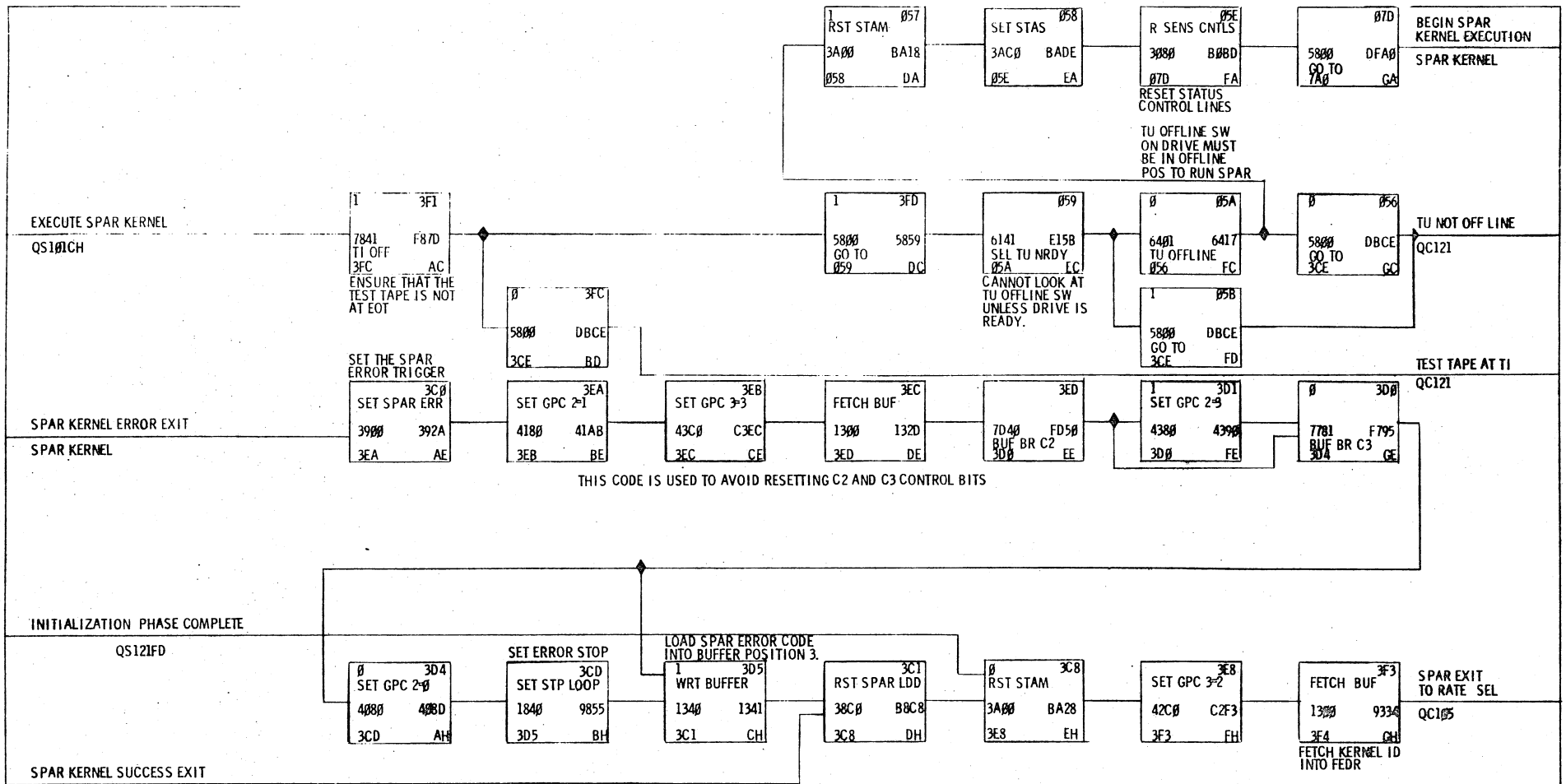
QN181


3480
Ø 4F2
SET GPC Ø=4
4400 4438
4F8 EA
4F8
SET GPC 1=A
4A40 CA49
4C9 FA
3430
1 4F3
SET GPC Ø=6
4600 4639
4F9 EC
4F9
SET GPC 1=6
4640 C649
4C9 FC
Ø 4FØ
7901 7933
MOD 3430
4F2 CC
3450
Ø 4F4
SET GPC Ø=5
4500 4539
4F9 EE
3460
1 4F5
SET GPC Ø=5
4500 C53B
4FB EG
4FB
SET GPC 1=2
4240 4249
4C9 FG
Ø 4CE
7581 75B1
MOD 3450/60
4FØ BG
1 4F1
7941 F975
MOD 3460
4F4 CG
GPC LOADED FOR 7TR 200 BPI
QN111
3440
Ø 4F6
SET GPC Ø=5
4500 453C
4FC EJ
4FC
SET GPC 1=E
4E40 4E49
4C9 FJ
3470
1 4F7
SET GPC Ø=4
4400 C43C
4FC EL
7TR 200 BPI
QN101CH
1 4C3
7981 F98F
MOD 3440/70
4CE AJ
1 4CF
7980 F9B6
MOD 3470
4F6 BL
QN105
20
LOAD NBCR FOR 200 BPI
PRESENT EC 22020
DATE 6-25-73
CD LOC
CD PN
PREV EC 22015
PG PN 31324
CD TYPE
MACH 3800-111
QN105



LOAD NBCR FROM GPC				
PRESENT E C	22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C	22Ø15	PG PN 31325	CD TYPE	MACH 38ØØ - 111


SPAR REQUEST
QS121ZE
IF STAS IS ON, WE ARE CURRENTLY DOING A SPAR COMMAND REQ.
1 287
7CC1 7CF3
STAS
2B2 BA
SPAR CMND REQ
QS121
MACH RST 2B2
398Ø B9B4
2B4 AB
RST GPC 2B4
Ø98Ø Ø9B5
2B5 BB
FETCH BUF 2B5
13ØØ 9338
2B8 CB
LOAD THE ADR REG
ING ADR, IOR 2B8
Ø18Ø 81B9
2B9 DB
SELECT THE DRIVE TO BE TESTED
SET TU SEL 2B9
Ø1ØØ Ø121
2A1 EB
2A1
58ØØ DBFE
GO TO
3FE FB
SET GPC 3=3 3FE
43CØ 43D8
3D8 BC
FETCH BUF 3D8
13ØØ 931A
3DA CC
S STA CTL=7 3DA
3ØØØ BØ42
3C2 DC
BITS C1, C2, and C3 OF BUFFER POSITION 3 PROVIDE SPAR RUN OPTIONS:
C1 C2 C3
Ø Ø Ø NORMAL RUN
Ø Ø 1 LOOP KERNEL
Ø 1 Ø SPACE FORWARD
Ø 1 1 LOOP TEST
1 1 Ø SEARCH AND STOP
1 1 1 SEARCH AND GO
DESIGN NOTE: THE MICRO ORDER 'S STA CTL=7' MUST BE ISSUED AT LEAST 2 MICRO SECONDS BEFORE INTERROGATING THE OFFLINE SWITCH.
SPACE
1 3C7
RST SPAR LDD
38CØ 38FØ
3FØ EE
SEARCH
1 3C5
RST SPAR LDD
38CØ 38FØ
3FØ BF
Ø 3F9
SET GPC 3=1
41CØ 41DF
3DF FF
FETCH BUF 3DF
13ØØ 932Ø
3E0 GF
FETCH THE ADR OF SPAR LOAD DRIVE.
3C2
7DØ1 FDØ5
BUF BR C1
3C4 AG
Ø 3C4
7781 F78B
BUF BR C3
3CA BG
Ø 3CA
7D4Ø 7D46
BUF BR C2
3C6 DG
NORMAL RUN
Ø 3C6
7C4Ø FCBØ
SPAR LDD
3FØ EG
LOOP
1 3CB
SET SPAR LDD
388Ø 38B1
3F1 CH
SPAR LDD INDICATES, IF ON, THAT SPAR KERNEL HAS BEEN SUCCESSFULLY LOADED AND INITIALIZED.
3FF
RST TU SEL
ØØ4Ø 8Ø6Ø
3E0 GH
NOT USED IN SPAR
EXECUTE SPAR KERNEL
QS111
SPAR RELOAD AFTER INITIALIZATION FROM SPAR KERNEL
LOAD ADR REG. IOR IS LOADED WITH GARBAGE, BECAUSE GATES ARE WRONG.
ING ADR, IOR 3E0
Ø18Ø 81A1
3E1 YK
SET TU SEL 3E1
Ø1ØØ Ø122
3E2 ZK
S STA CTL=7 3E2
3ØØØ 3Ø4C
3CC AK
SET STATUS CONTROL LINE 2 ON. THIS WILL CAUSE TU OFFLINE SWITCH TO BE RETURNED TO TCU ON MOD LINE 2.
DELAY 3CC
58ØØ DBF8
3F8 BK
DELAY 3F8
58ØØ 5B93
GO TO 393 CK
TEST TO ENSURE THAT DRIVE IS OFFLINE.
Ø 3D2
6401 6427
TU OFFLINE
3E6 DK
RESET THE STATUS CONTROL LINES.
1 3E7
R SENS CNTLS
3ØØØ BØB2
3E2 EK
LOAD THE SPAR KERNEL. MICRO-PGM CONTROL WILL BE DISABLED UNTIL LOAD IS COMPLETE.
START LOAD 3F2
3A4Ø 3A57
3D7 FK
KERNEL LOADED
QS121
DELAY 393
58ØØ 5BF9
393 ZI
SET GPC 3=2 3F9
42CØ 42D6
3D6 AL
LOAD KERNEL TO FEBR.
FETCH BUF 3D5
13ØØ 9337
3E7 BL
6141 6153
SEL TU NRDY
3D2 CL
CANNOT LOOK AT TU OFFLINE SW IF TU NRDY IS INDICATED
1 3D3
58ØØ DBCE
3CE DL
Ø 3E6
58ØØ DBCE
3CE EL
TU NOT OFFLINE
QC121
PM1Ø17
QSIG
SPAR KERNEL LOAD
PRESENT E C 22Ø1
DATE 1Ø/31/74
CD LOC
CD PN
PREV E C 22ØØ
PG PN 32ØØ CD 4
CD TYPE
MACH 38ØØ-111
QSIG



STAS A SPAR KERNEL CAN LOAD COMMANDS INTO THE BUFFER AND THEN HAVE THEM BE EXECUTED BY THE MICRO-PROGRAM. STAS IS USED TO CONTROL THE OPTIONAL RETURN TO THE IDLE LOOP. IF STAS IS OFF AS A BUFFER COMMAND COMPLETES, THE IDLE LOOP IS BYPASSED, AND ANOTHER COMMAND IS IMMEDIATELY ACCESSED. THUS THE SPAR KERNEL CAN ALLOW THE CPU TO BREAK IN-BETWEEN THESE COMMANDS BY LEAVING STAS SET, OR CAN INSURE THAT CPU DOES NOT BREAK IN AFTER A COMMAND BY RESETTING STAS.

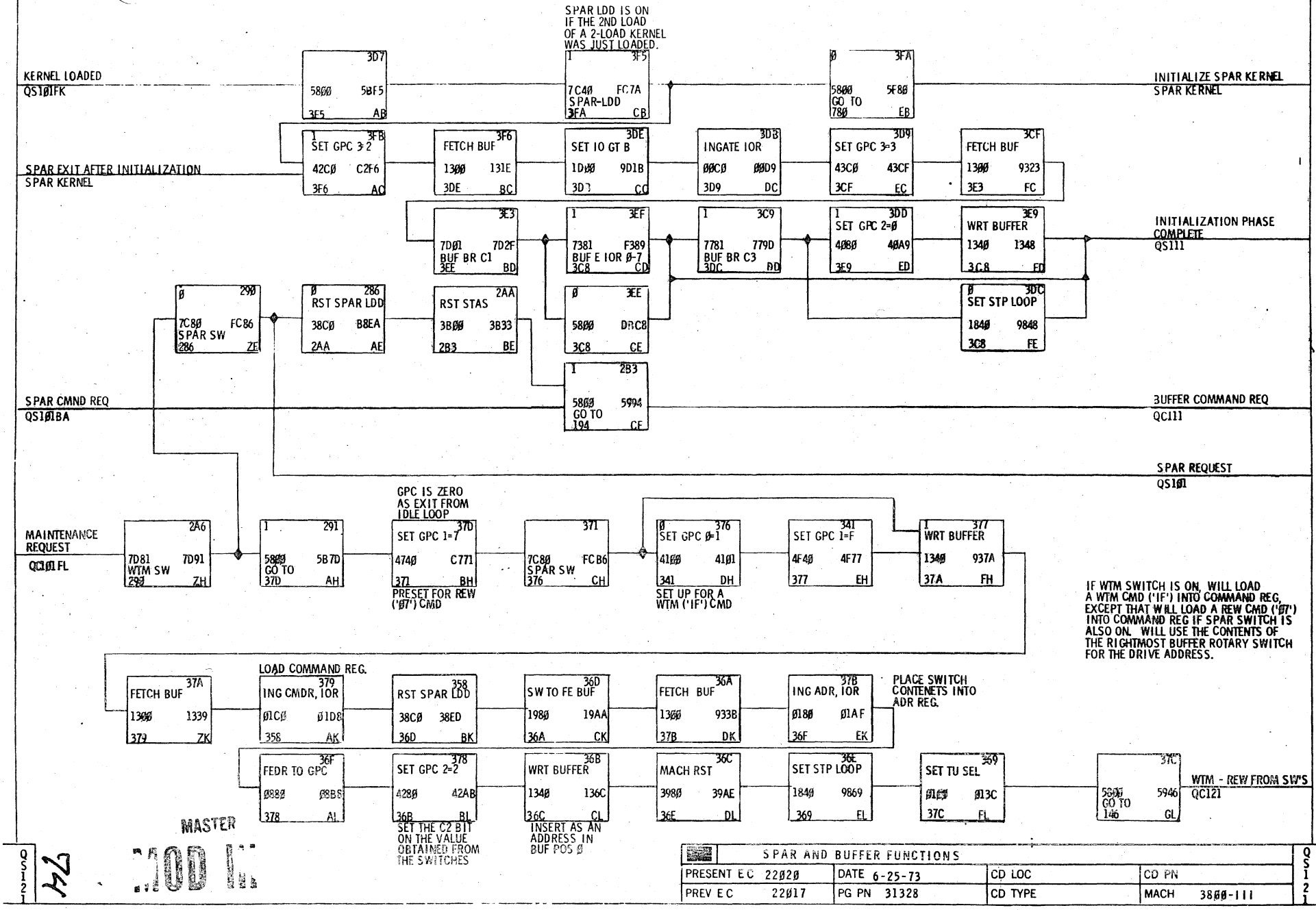
STAM THE SPAR KERNEL CAN USE THE LOAD BCR ROUTINE OF THE MICRO-PGM, WHICH IS ENTERED AT BLOCK 1ØØ ON QM121. STAM, IF ON, CAUSES A RETURN TO LOCATION 7BØ OF THE SPAR KERNEL AFTER THE BCR IS LOADED. IF STAM IS OFF, BUFFER COMMANDS EXECUTED FOR A SPAR KERNEL WILL BE PERFORMED NORMALLY.
STAM IS ALSO USED AS A BUFFER CHAIN COMMAND CONTROL. IF A '4B' COMMAND IS ISSUED IT WILL SET STAM. A TIO ('ØØ') WILL RESET STAM. IF STAM IS ON AS A BUFFER COMMAND IS COMPLETED, THE IDLE LOOP IS BYPASSED AND ANOTHER COMMAND FROM THE BUFFER IS IMMEDIATELY ACCESSED.

PM1Ø17

SPAR KERNEL ENTRY AND EXITS				
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
[illegible] EC 22Ø15	PG PN [illegible]327	CD TYPE	MACH 38ØØ - [illegible]	

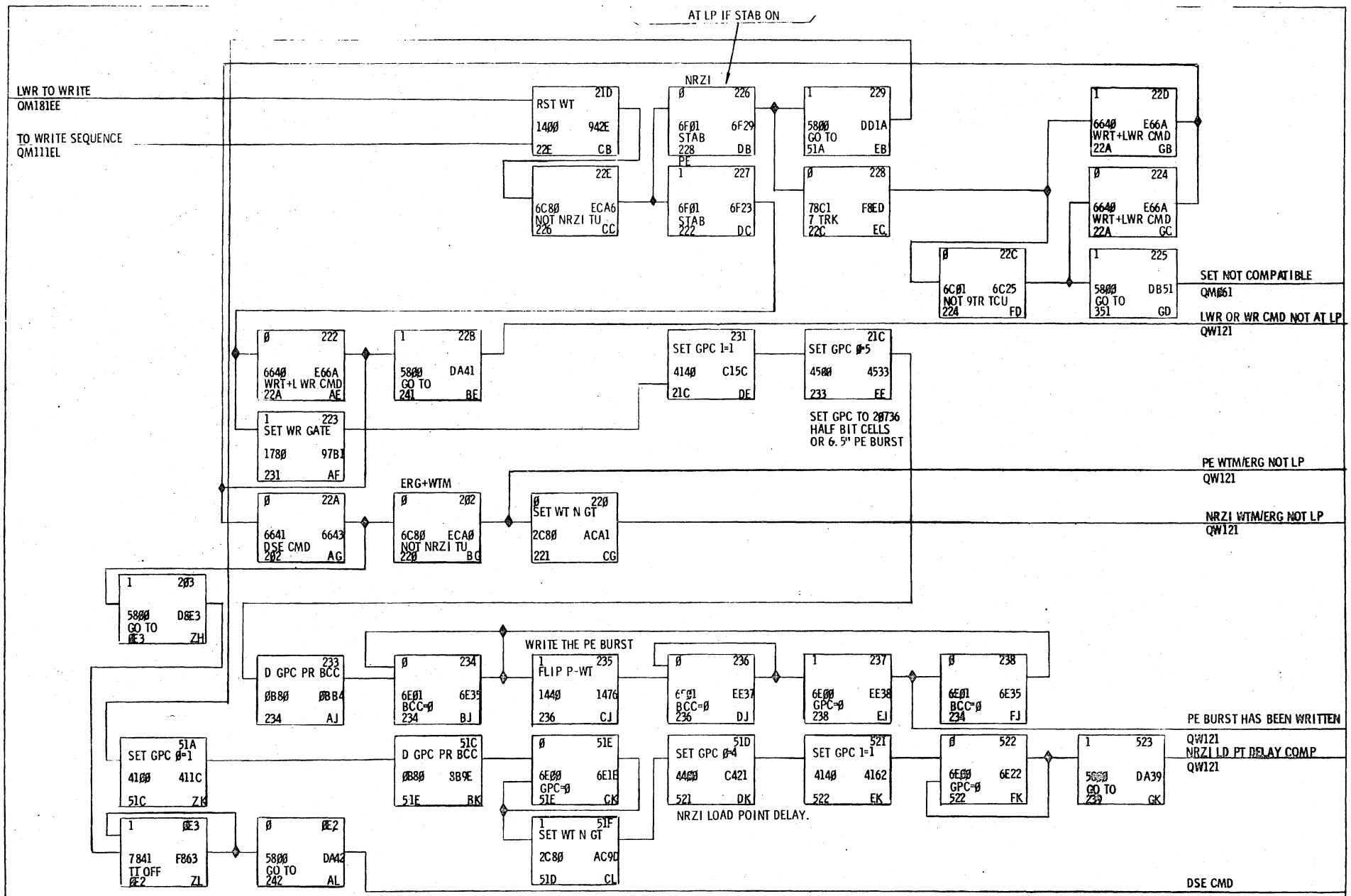
QS111 — QS111

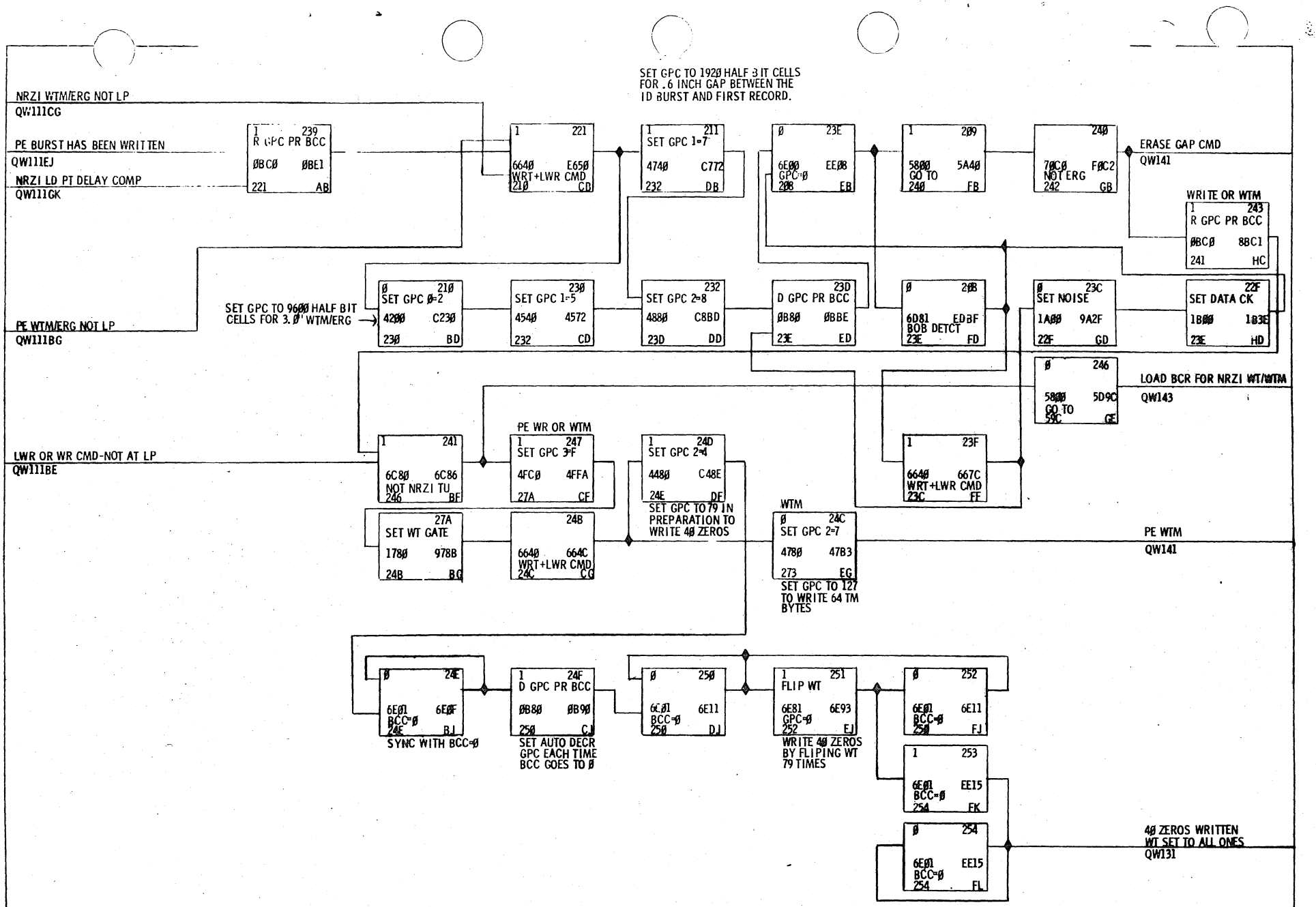
MASTER



SPAR AND BUFFER FUNCTIONS			
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV E C 22Ø17	PG PN 31328	CD TYPE	MACH 38ØØ-111

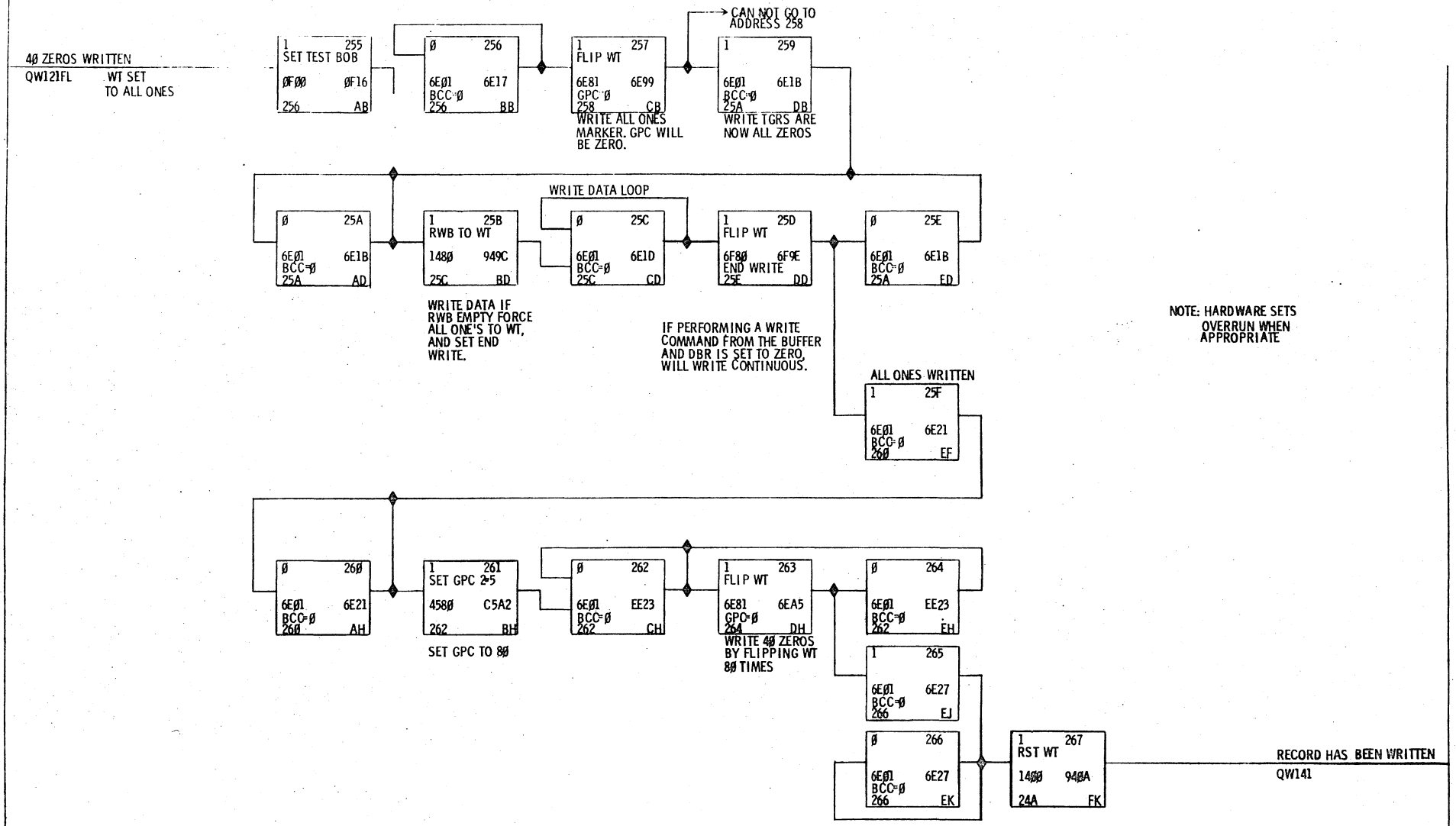
QS121 QS121


AT LP IF STAB ON
LWR TO WRITE
QM181EE
TO WRITE SEQUENCE
QM111EL
NRZI
RST WT
1400 942E
22E CB
6F01 6F29
STAB
228 DB
PE
6F01 6F23
STAB
222 DC
6C80 ECA6
NOT NRZI TU
226 CC
5800 DD1A
GO TO
51A EB
78C1 F8ED
7 TRK
22C EC
6640 E66A
WRT+LWR CMD
22A GB
6640 E66A
WRT+LWR CMD
22A GC
6C01 6C25
NOT 9TR TCU
224 FD
5800 DB51
GO TO
351 GD
SET NOT COMPATIBLE
QM861
LWR OR WR CMD NOT AT LP
QW121
6640 E66A
WRT+L WR CMD
22A AE
5800 DA41
GO TO
241 BE
SET GPC 1=1
4140 C15C
21C DE
SET GPC 0=5
4500 4533
233 EE
SET GPC TO 2#736
HALF BIT CELLS
OR 6.5" PE BURST
SET WR GATE
1780 97B1
231 AF
PE WTM/ERG NOT LP
QW121
ERG+WTM
6641 6643
DSE CMD
202 AG
6C80 ECA0
NOT NRZI TU
220 BG
SET WT N GT
2C80 ACA1
221 CG
NRZI WTM/ERG NOT LP
QW121
5800 D0E3
GO TO
0E3 ZH
WRITE THE PE BURST
D GPC PR BCC
0B80 0BB4
234 AJ
6E01 6E35
BCC=0
234 BJ
FLIP P-WT
1440 1476
236 CJ
6E01 EE37
BCC=0
236 DJ
6E00 EE38
GPC=0
238 EJ
6E01 6E35
BCC=0
234 FJ
PE BURST HAS BEEN WRITTEN
QW121
NRZI LD PT DELAY COMP
QW121
SET GPC 0=1
4100 411C
51C ZK
D GPC PR BCC
0B80 8B9E
51E BK
6E00 6E1E
GPC=0
51E CK
SET GPC 0=4
4400 C421
521 DK
SET GPC 1=1
4140 4162
522 EK
6E00 6E22
GPC=0
522 FK
5800 DA39
GO TO
239 GK
NRZI LOAD POINT DELAY.
7841 F863
TT OFF
0E2 ZL
5800 DA42
GO TO
242 AL
SET WT N GT
2C80 AC9D
51D CL
DSE CMD
QW141
ENTRY TO WRITE AND WRITE PE BURST
PRESENT EC 22020
DATE 6-25-73
CD LOC
CD PN
EC 22015
PG PN
CD TYPE
MACH 3800-
QW111
QW111
25



GAP AFTER PE BURST AND WRITE 4Ø ZEROS			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
PREV EC 22Ø15	PG PN 3133Ø	CD TYPE	MACH 38ØØ-111

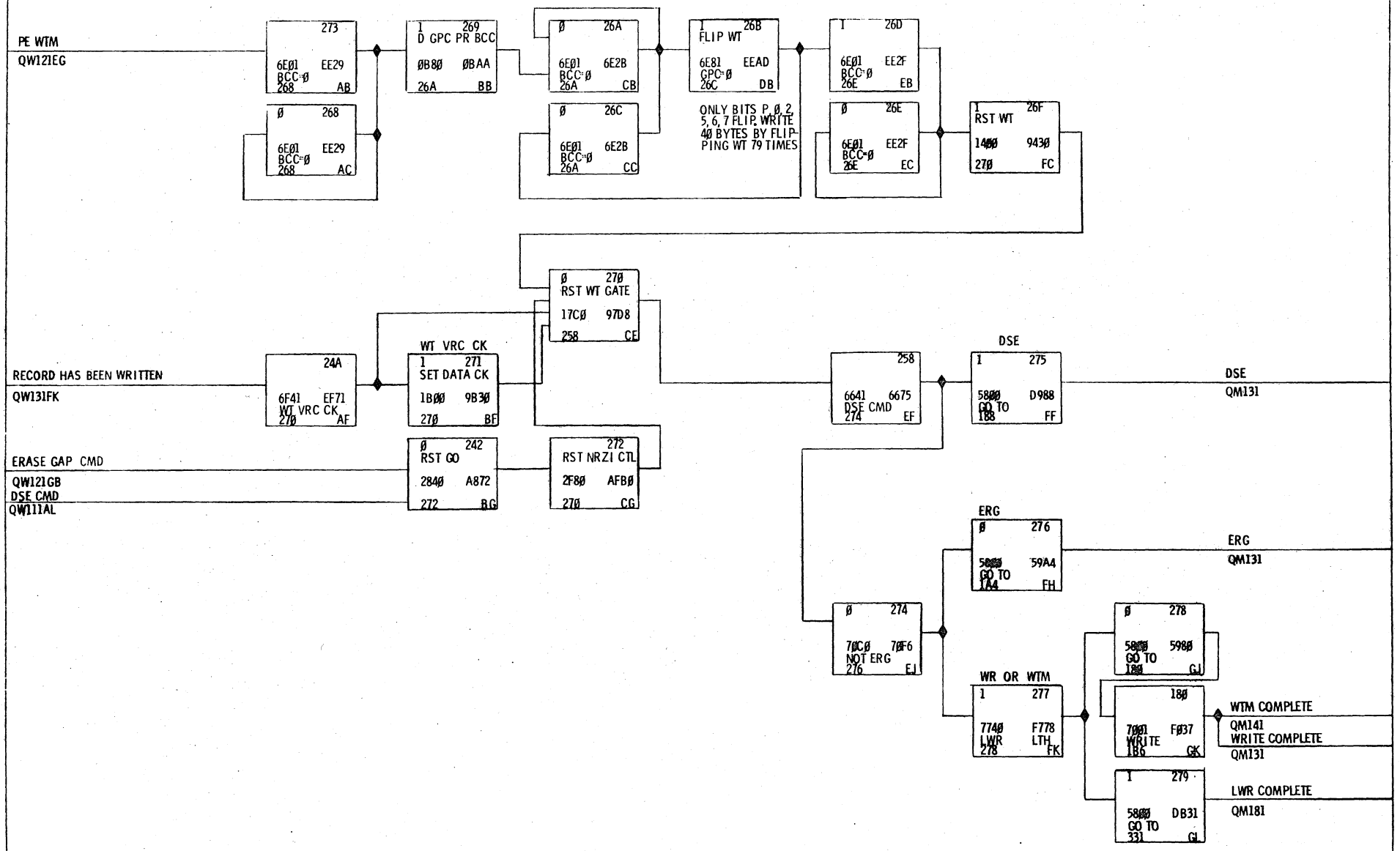
QW121 92 QW121



MASTER

MOD III

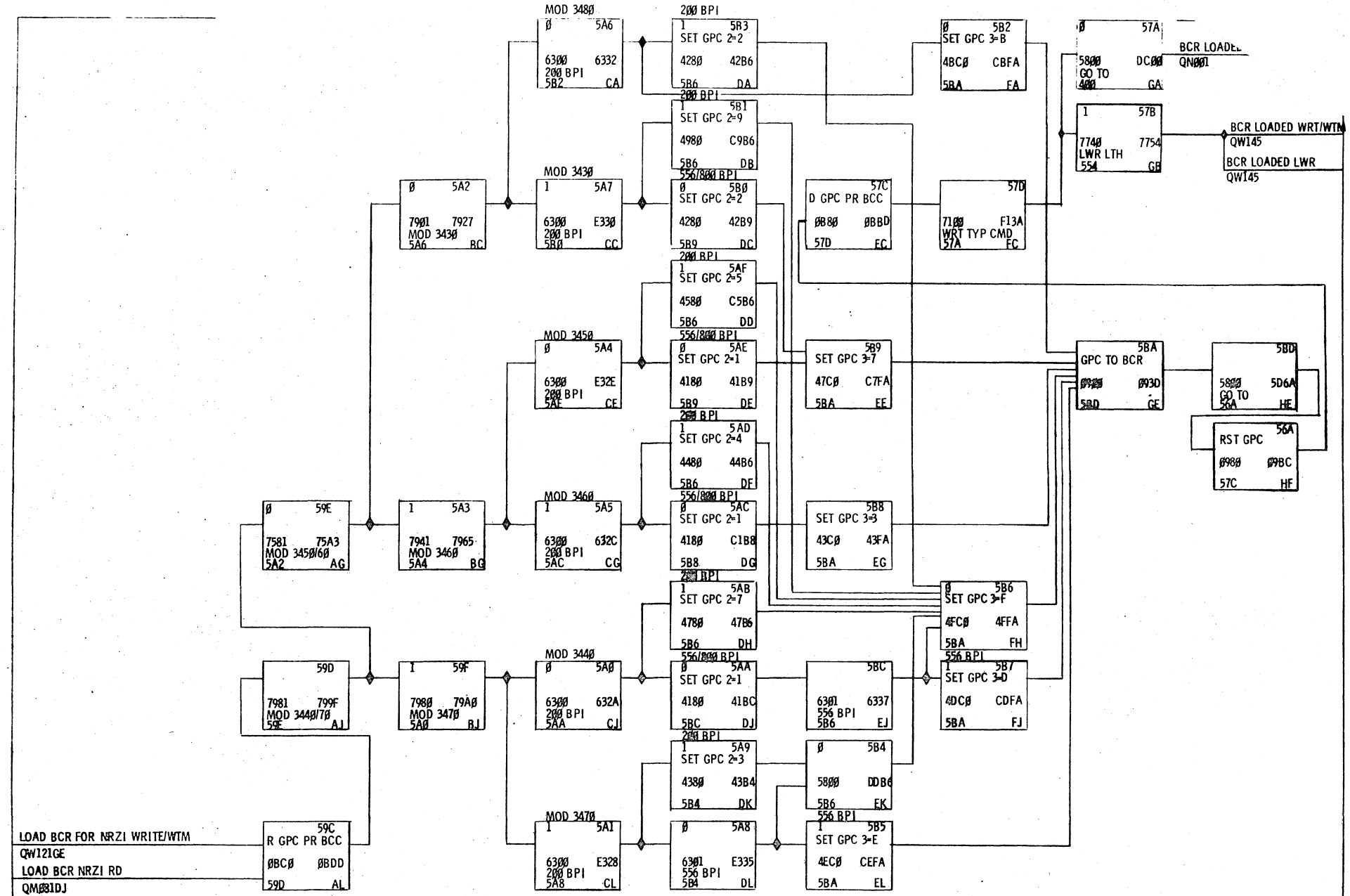
QW131	PE WRITE DATA			QW131
PRESENT EC 22Ø15	DATE 6-29-72	CD LOC	CD PN	
PREV EC 22ØØ1	PG PN 2255Ø	CD TYPE	MACH 38ØØ-111	



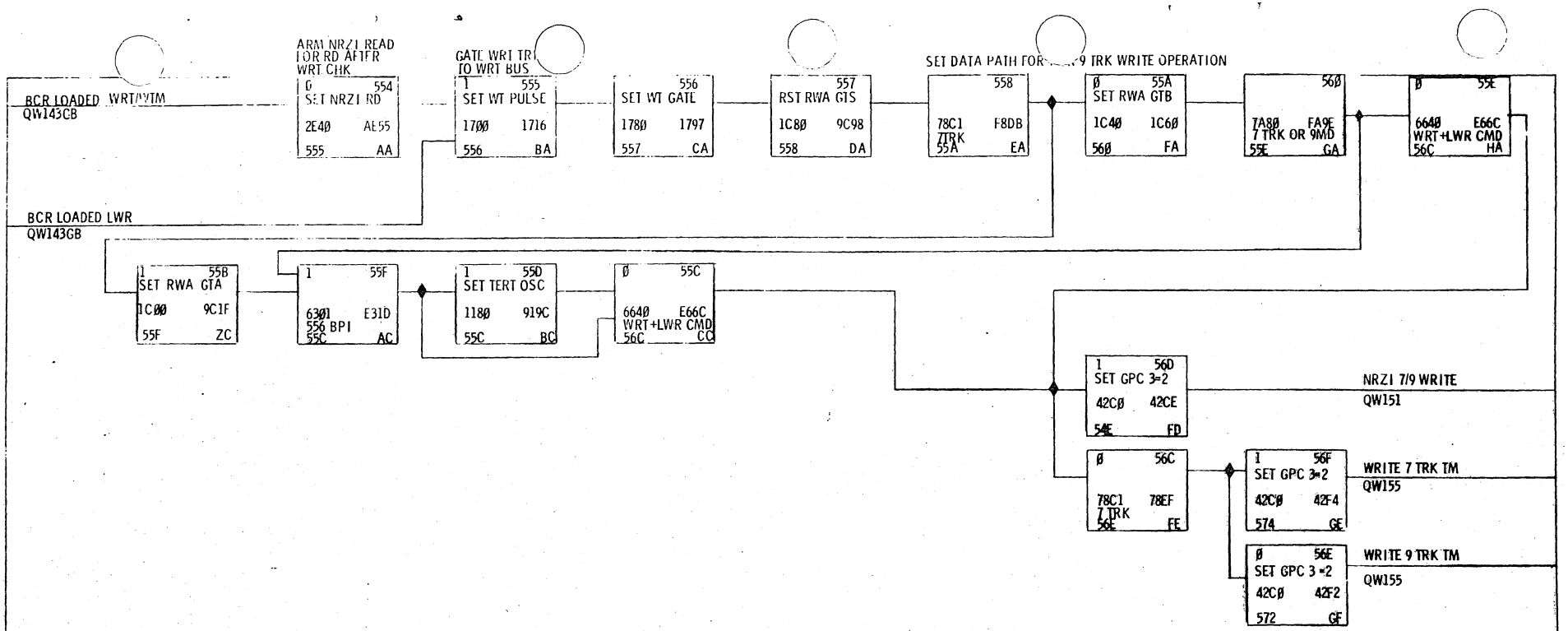
MASTER
MOD III

PE WTM AND WRITE ENDING			
PRESENT E C 22ØØ4	DATE 1-4-72	CD LOC	CD PN
PREV E C	PG PN 22551	CD TYPE	MACH 38ØØ-111

QW141 82 QW141



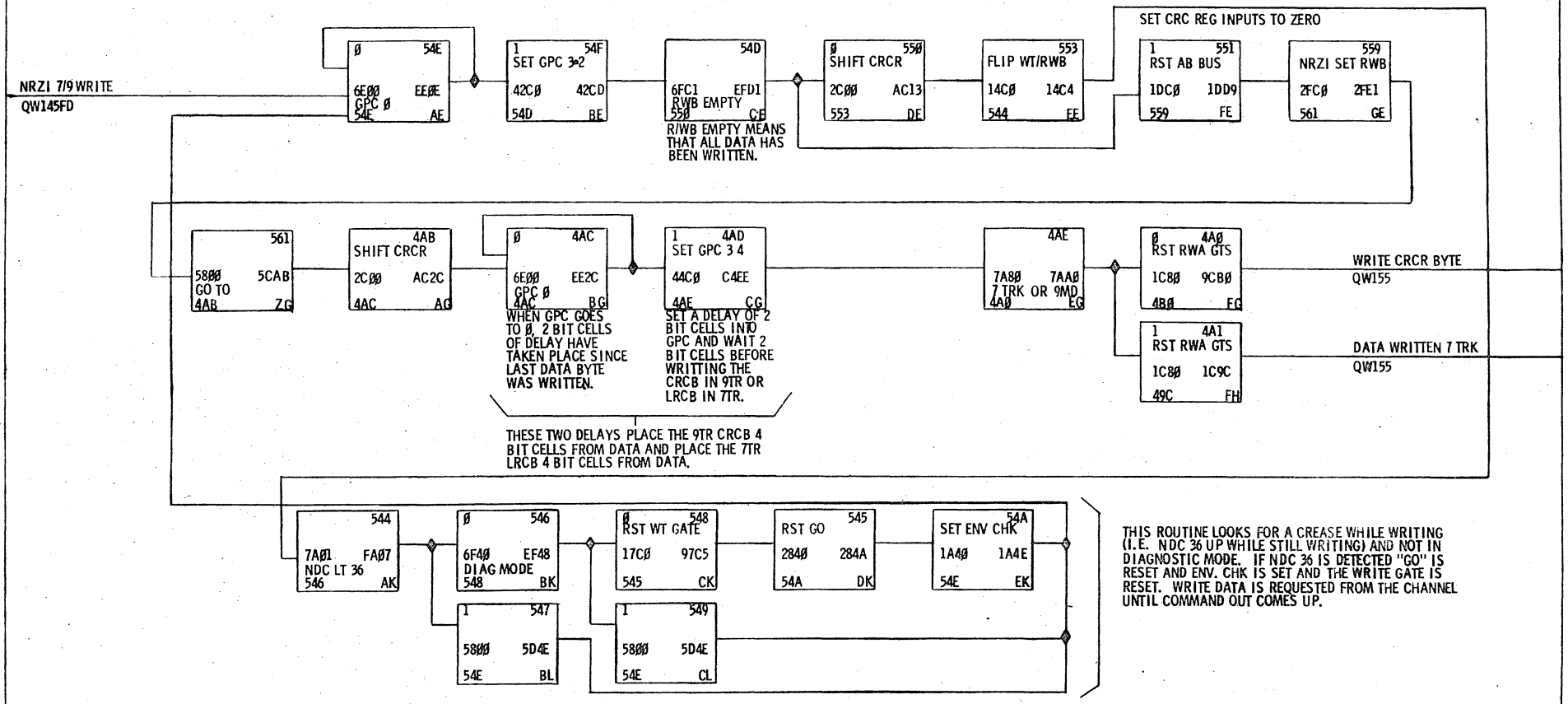
QWI43	LOAD BCR FOR NRZI WRITE			QWI43
PRESENT E C 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN	
E C 22Ø15	PG PN	CD TYPE	MACH 38ØØ-	



QW145	SET BCR FOR 7TR 200 BPI WRITE			QW145
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22015	PG PN 31332	CD TYPE	MACH 3800-111	

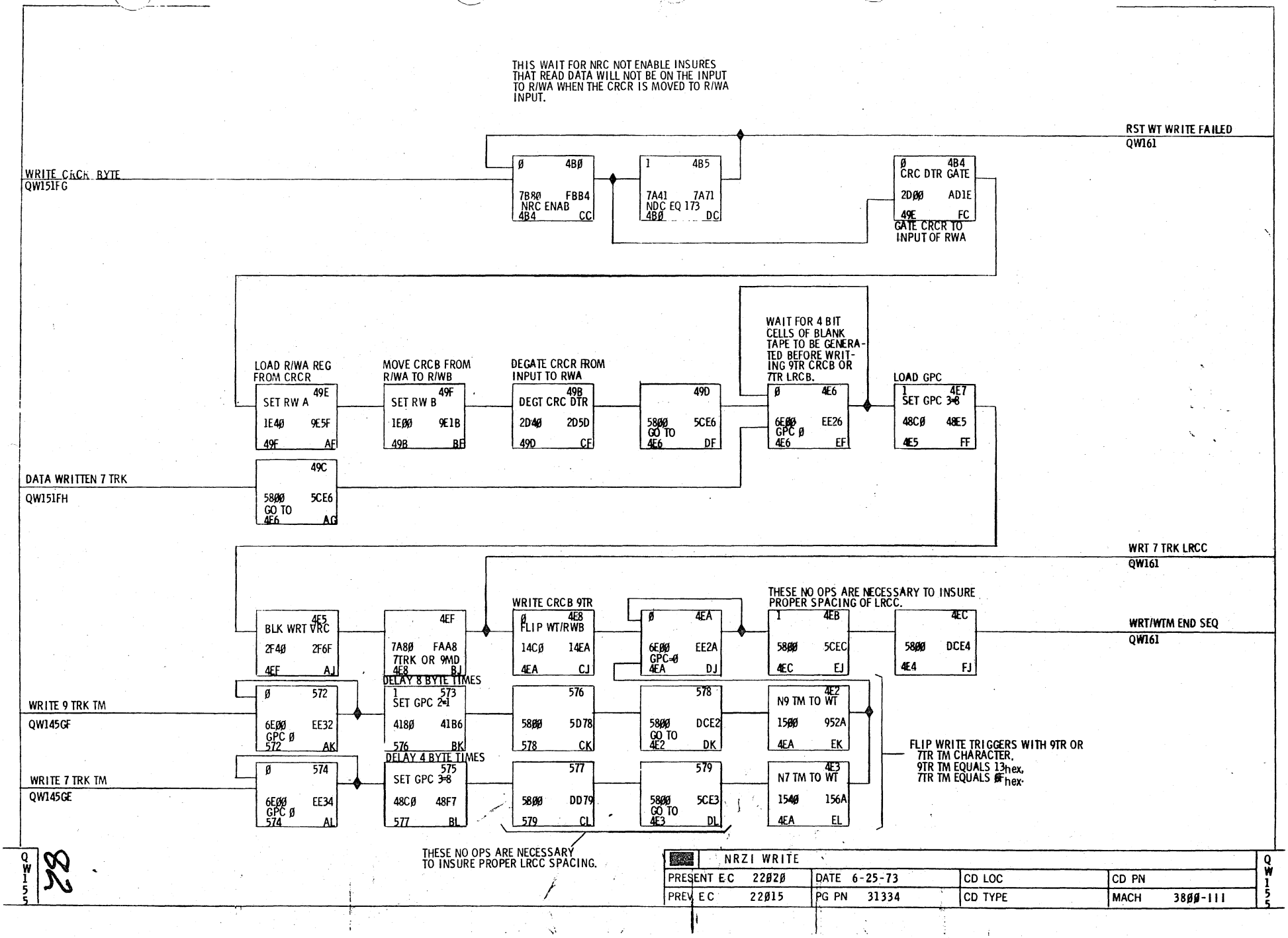
89

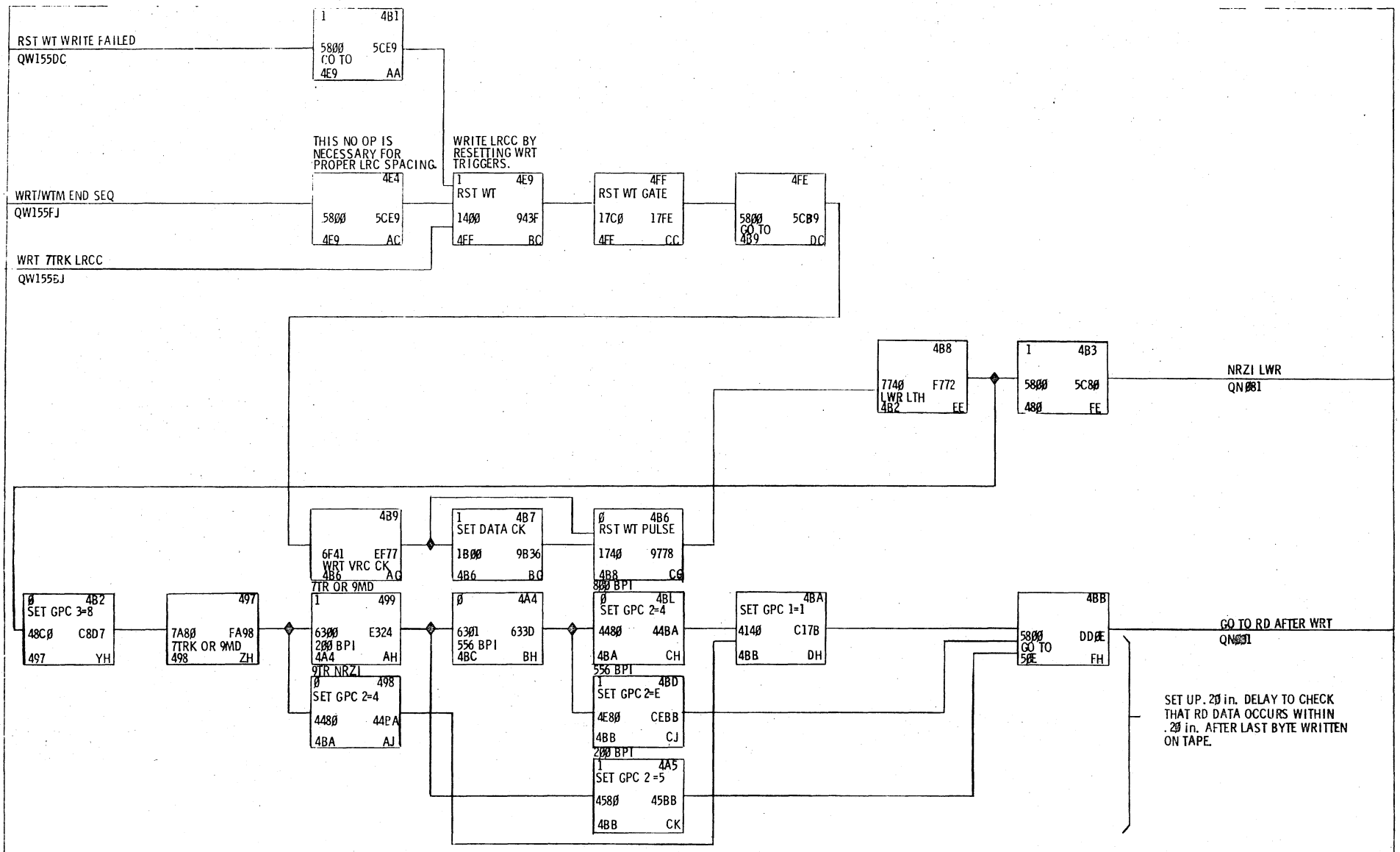
NRZI WRITE (7 OR 9 TRACK). A VALUE IS LOADED INTO THE BCR WHICH IS EQUAL TO 1/2 THE BIT CELL. THIS VALUE IN TURN IS LOADED INTO THE BCC WHEN EVER THE BCC GOES TO ZERO. ALSO THE GPC IS LOADED LOADED WITH 2 AND EVERYTIME THE BCC GOES TO ZERO THE GPC IS DEC.



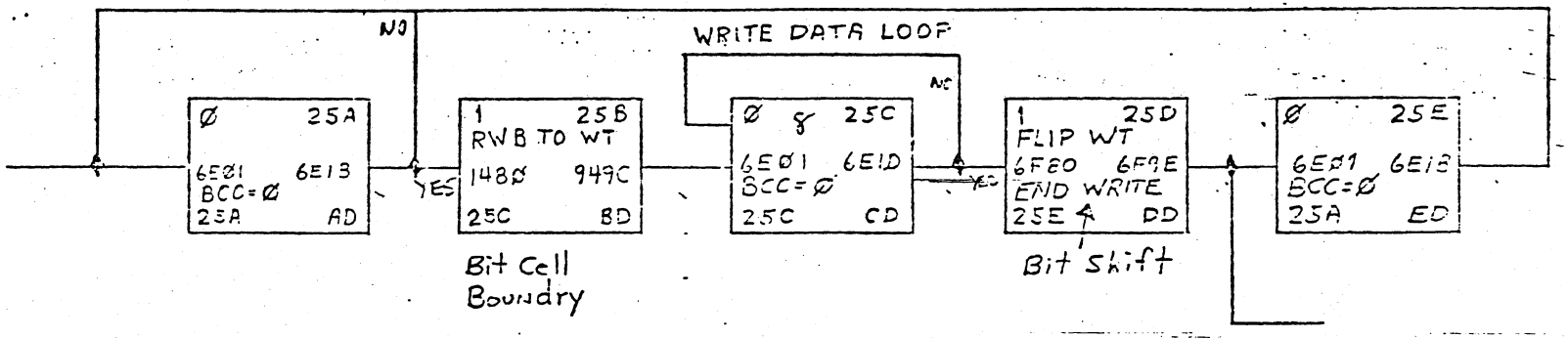
NRZI WRITE			
PRESENT EC 22Ø2Ø	DATE 6-25-73	CD LOC	CD PN
EC 22Ø15	PG PN	CD TYPE	MACH 38ØØ-

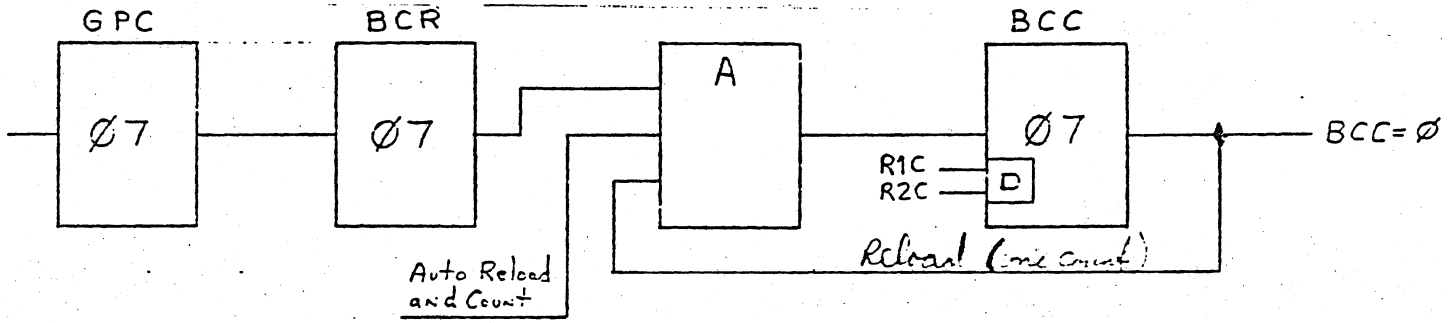
QW151


THIS WAIT FOR NRC NOT ENABLE INSURES THAT READ DATA WILL NOT BE ON THE INPUT TO R/WA WHEN THE CRCR IS MOVED TO R/WA INPUT.
RST WT WRITE FAILED
QW161
WRITE CRCR BYTE
QW151FG
Ø 4BØ
7B8Ø FBB4
NRC ENAB
4B4 CC
1 4B5
7A41 7A71
NDC EQ 173
4BØ DC
Ø 4B4
CRC DTR GATE
2DØØ AD1E
49E FC
GATE CRCR TO INPUT OF RWA
LOAD R/WA REG FROM CRCR
49E
SET RW A
1E4Ø 9E5F
49F AF
MOVE CRCB FROM R/WA TO R/WB
49F
SET RW B
1EØØ 9E1B
49B BF
DEGATE CRCR FROM INPUT TO RWA
49B
DEGT CRC DTR
2D4Ø 2D5D
49D CF
49D
58ØØ 5CE6
GO TO
4E6 DF
WAIT FOR 4 BIT CELLS OF BLANK TAPE TO BE GENERATED BEFORE WRITING 9TR CRCB OR 7TR LRCB.
Ø 4E6
6EØØ EE26
GPC Ø
4E6 EF
LOAD GPC
1 4E7
SET GPC 3=8
48CØ 48E5
4E5 FF
DATA WRITTEN 7 TRK
QW151FH
49C
58ØØ 5CE6
GO TO
4E6 AG
WRT 7 TRK LRCC
QW161
WRITE CRCB 9TR
Ø 4E8
FLIP WT/RWB
14CØ 14EA
4EA CJ
THESE NO OPS ARE NECESSARY TO INSURE PROPER SPACING OF LRCC.
Ø 4EA
6EØØ EE2A
GPC-Ø
4EA DJ
1 4EB
58ØØ 5CEC
4EC EJ
4EC
58ØØ DCE4
4E4 FJ
WRT/WTM END SEQ
QW161
4E5
BLK WRT VRC
2F4Ø 2F6F
4EF AJ
4EF
7A8Ø FAA8
7TRK OR 9MD
4E8 BJ
DELAY 8 BYTE TIMES
1 573
SET GPC 2=1
418Ø 41B6
576 BK
WRITE 9 TRK TM
QW145GF
Ø 572
6EØØ EE32
GPC Ø
572 AK
576
58ØØ 5D78
578 CK
578
58ØØ DCE2
GO TO
4E2 DK
4E2
N9 TM TO WT
15ØØ 952A
4EA EK
DELAY 4 BYTE TIMES
575
SET GPC 3=8
48CØ 48F7
577 BL
WRITE 7 TRK TM
QW145GE
Ø 574
6EØØ EE34
GPC Ø
574 AL
577
58ØØ DD79
579 CL
579
58ØØ 5CE3
GO TO
4E3 DL
4E3
N7 TM TO WT
154Ø 156A
4EA EL
FLIP WRITE TRIGGERS WITH 9TR OR 7TR TM CHARACTER.
9TR TM EQUALS 13hex.
7TR TM EQUALS 8Fhex.
THESE NO OPS ARE NECESSARY TO INSURE PROPER LRCC SPACING.
NRZI WRITE
PRESENT EC 22Ø2Ø
DATE 6-25-73
CD LOC
CD PN
PREV EC 22Ø15
PG PN 31334
CD TYPE
MACH 38ØØ-111
QW155
QW155



NRZI WRITE.				
PRESENT E C 22020	DATE 6-25-73	CD LOC	CD PN	
PREV E C 22015	PG PN 31335	CD TYPE	MACH 3800-III	



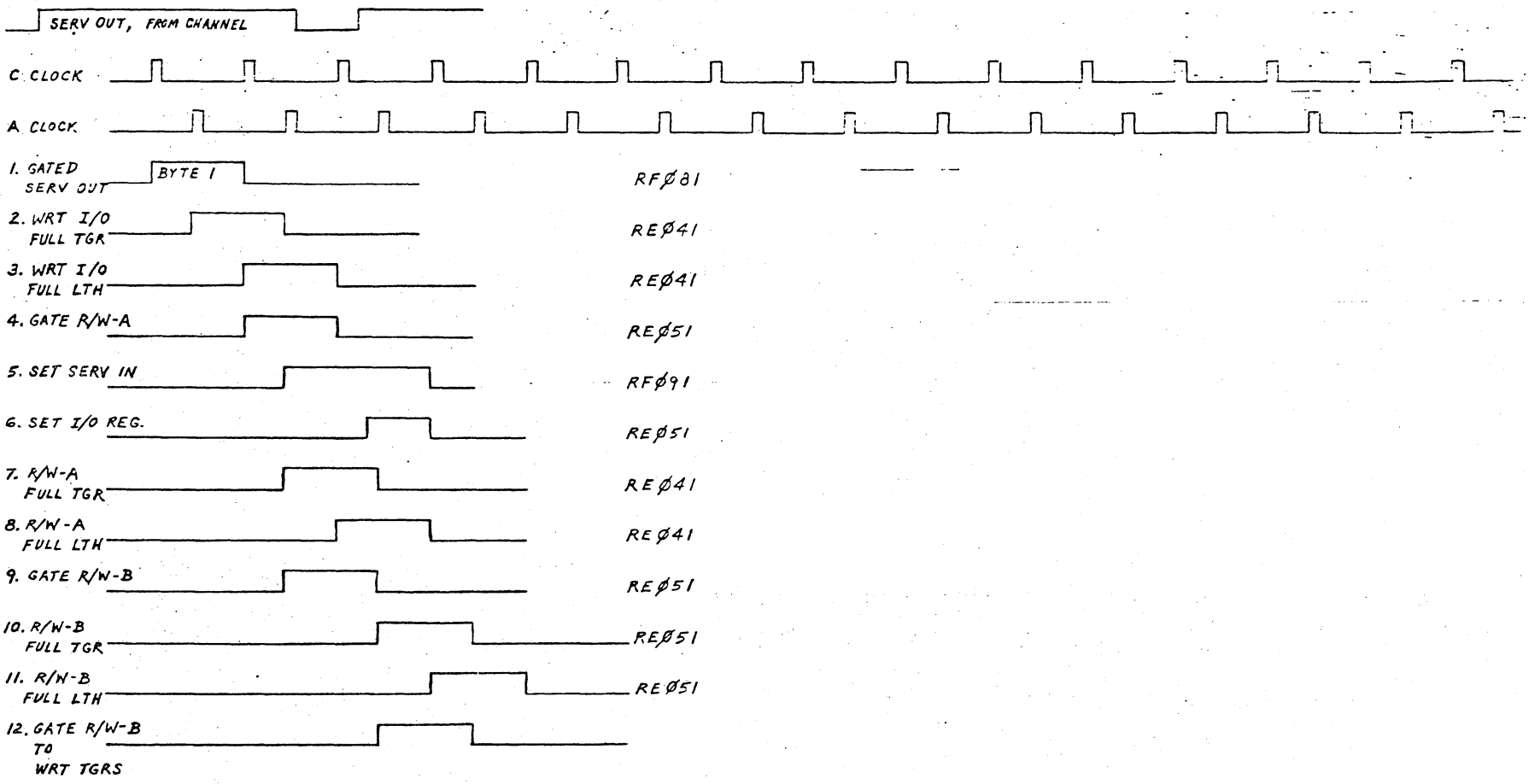


3470 Bit Cell Timing

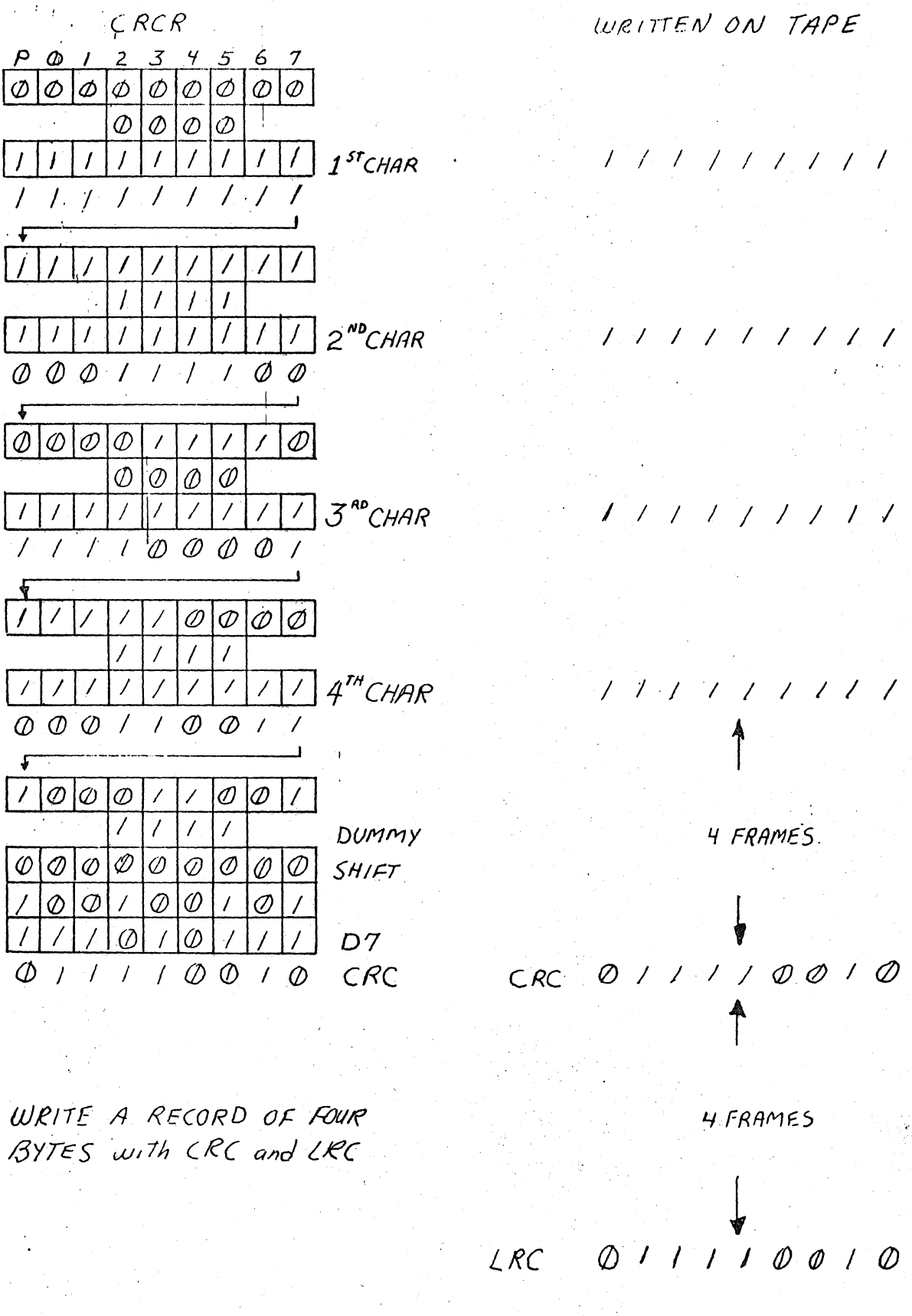
A 3470 moves tape at 200 ips
PE is written at 1600 bpi
∴ 320,000 bits are written/sec
giving a bit cell time of 3.12 μsec

H8

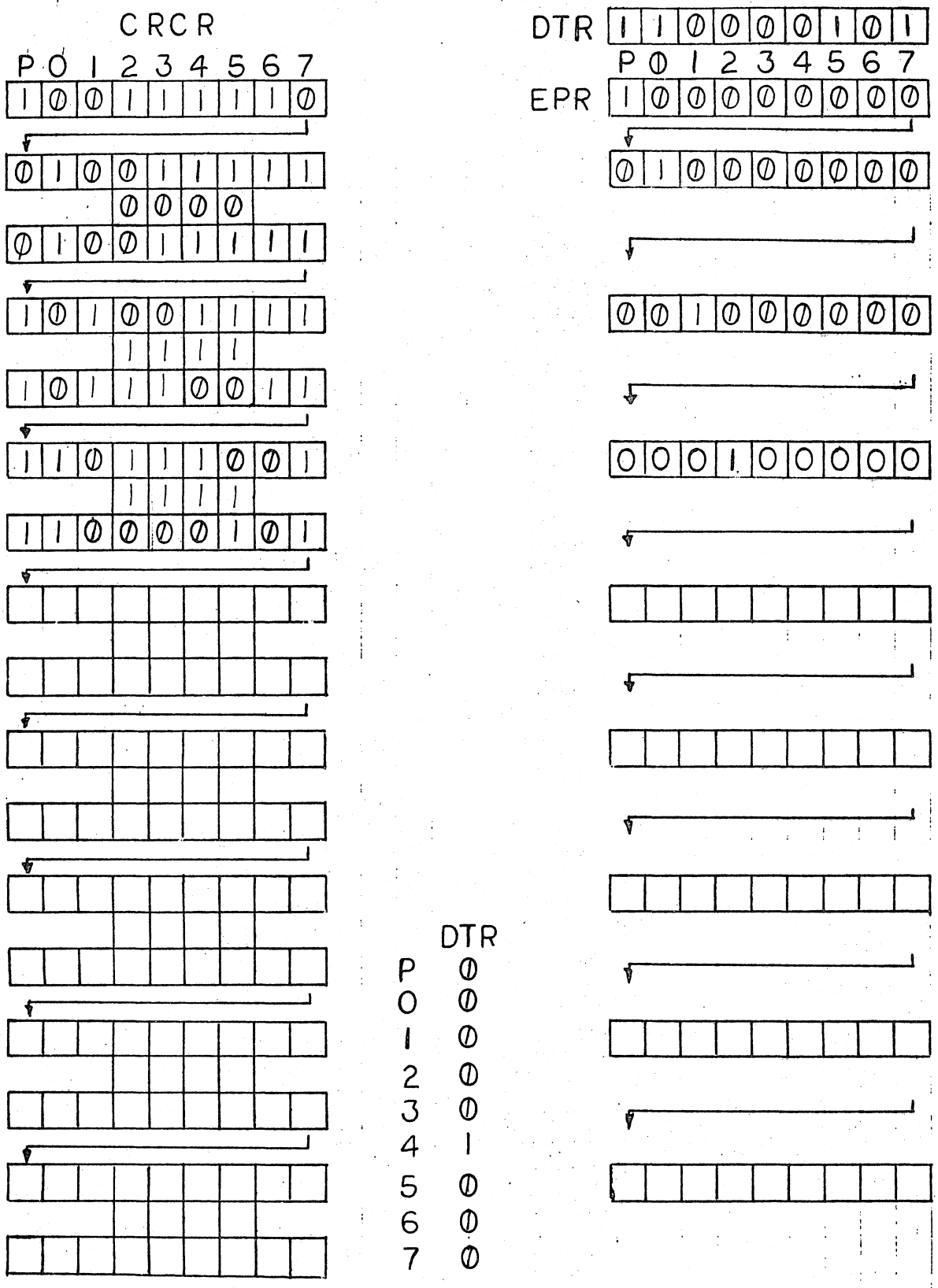
PE Write



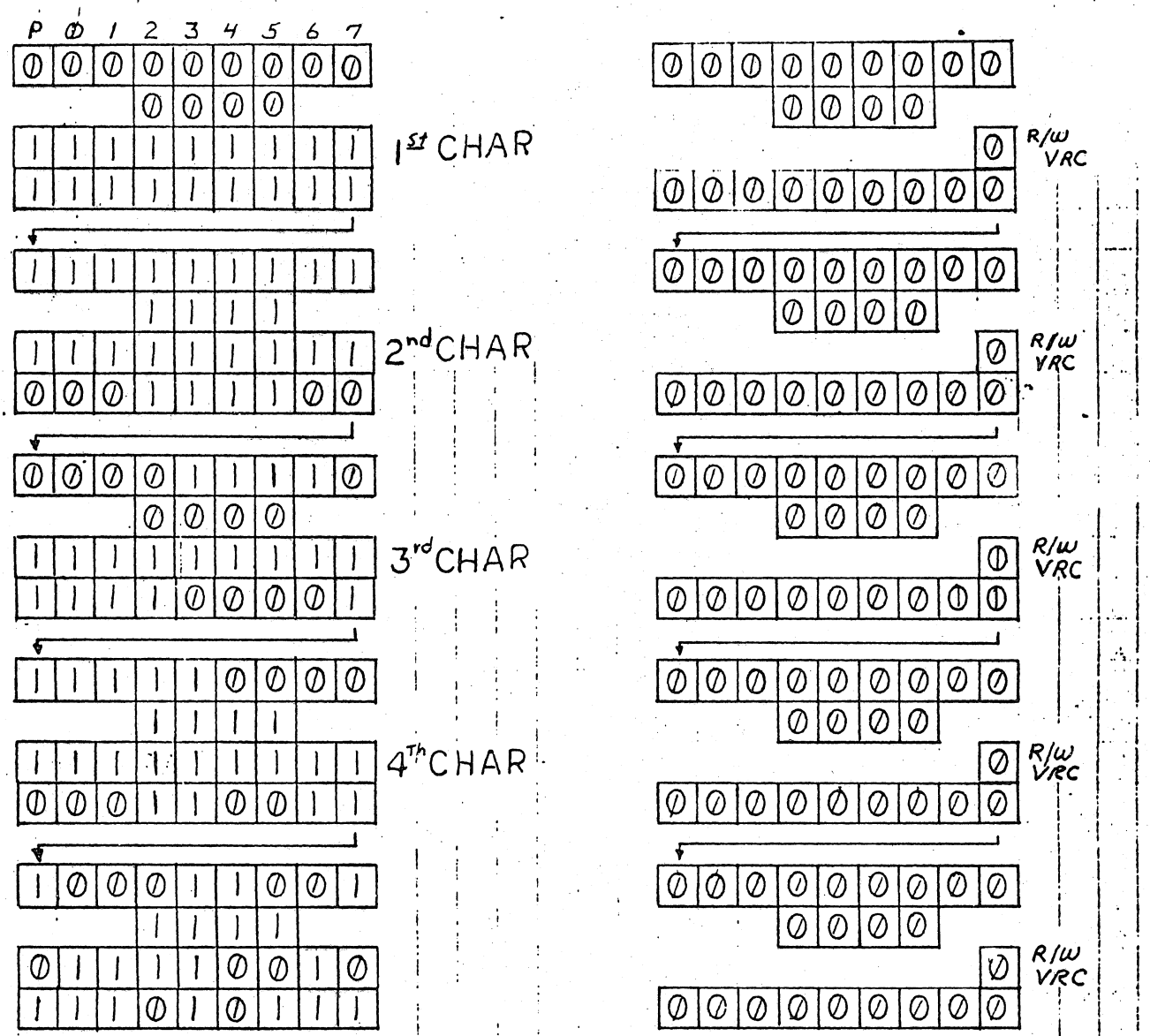
Write Timings.



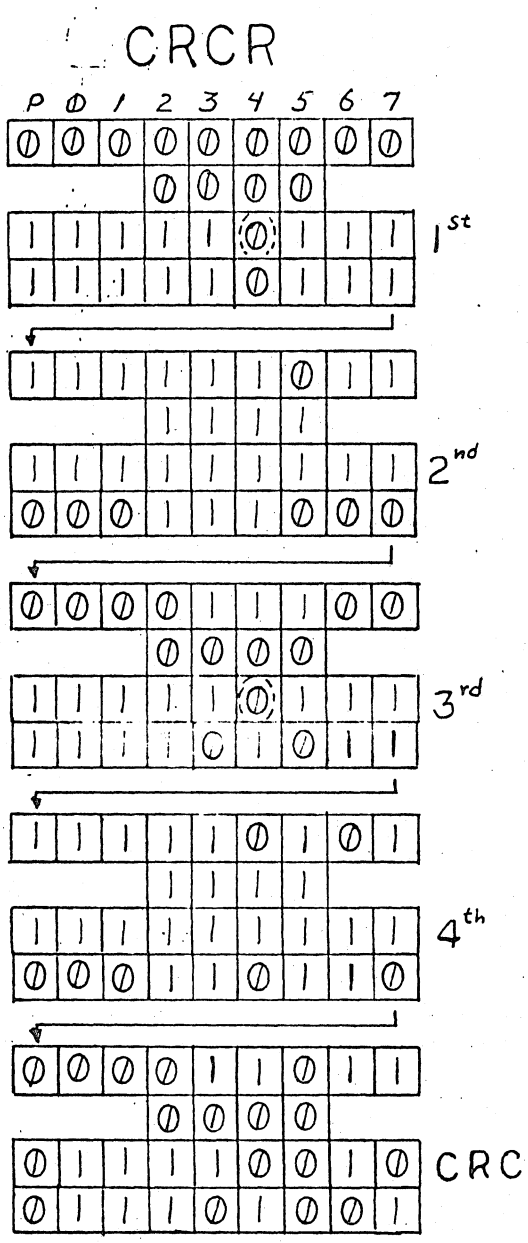
WRITE A RECORD OF FOUR BYTES with CRC and LRC



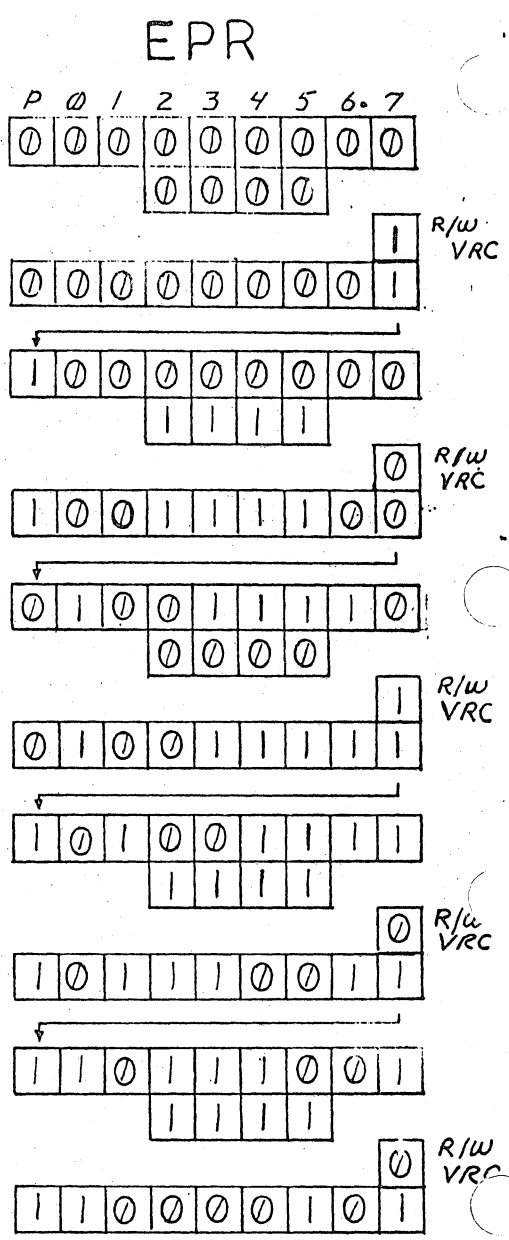
When CRC=DTR the track in Error (TIE) has been found (FOUND TRACK FF is Se
If FOUND is set on Read Forward the EPR is transferred in Reverse to the L
on a Read Backward the EPR is gated in a normal manner to the DTR.



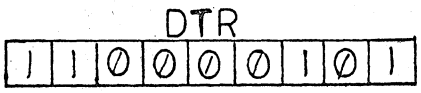
AT THE END OF A READ OR READ BACKWARD, THE CRC REGISTER SHOULD CONTAIN 111010111. THIS IS THE MATCH PATTERN.

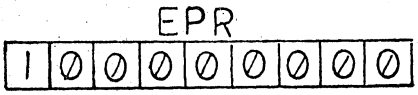


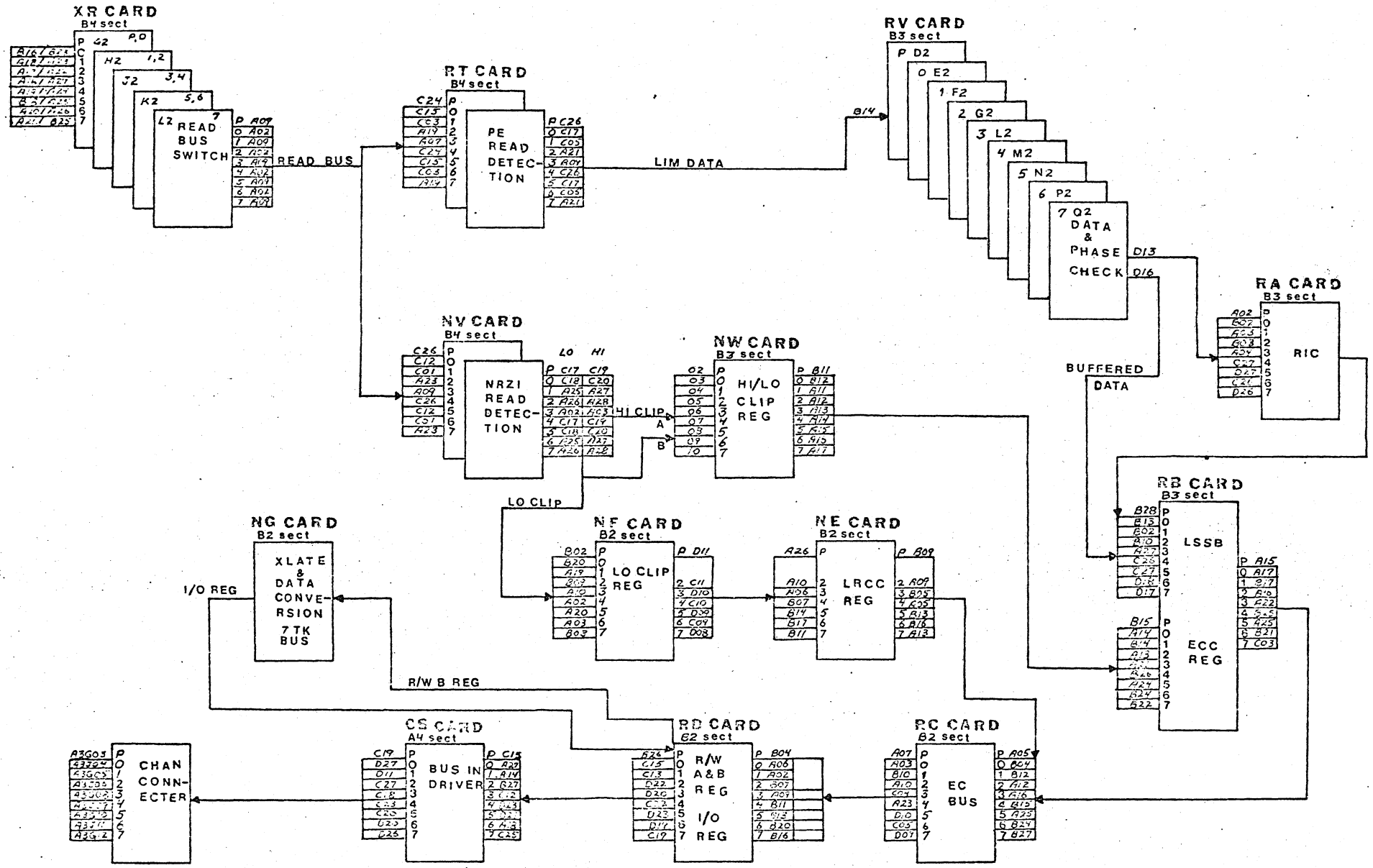
CRC register is complemented, except for bits 2 and 4, and compared to the DTR



The EPR is gated to the DTR. The EPR is reset and the P bit is turned on.







NRZI & PE READ DATA FLOW TX01

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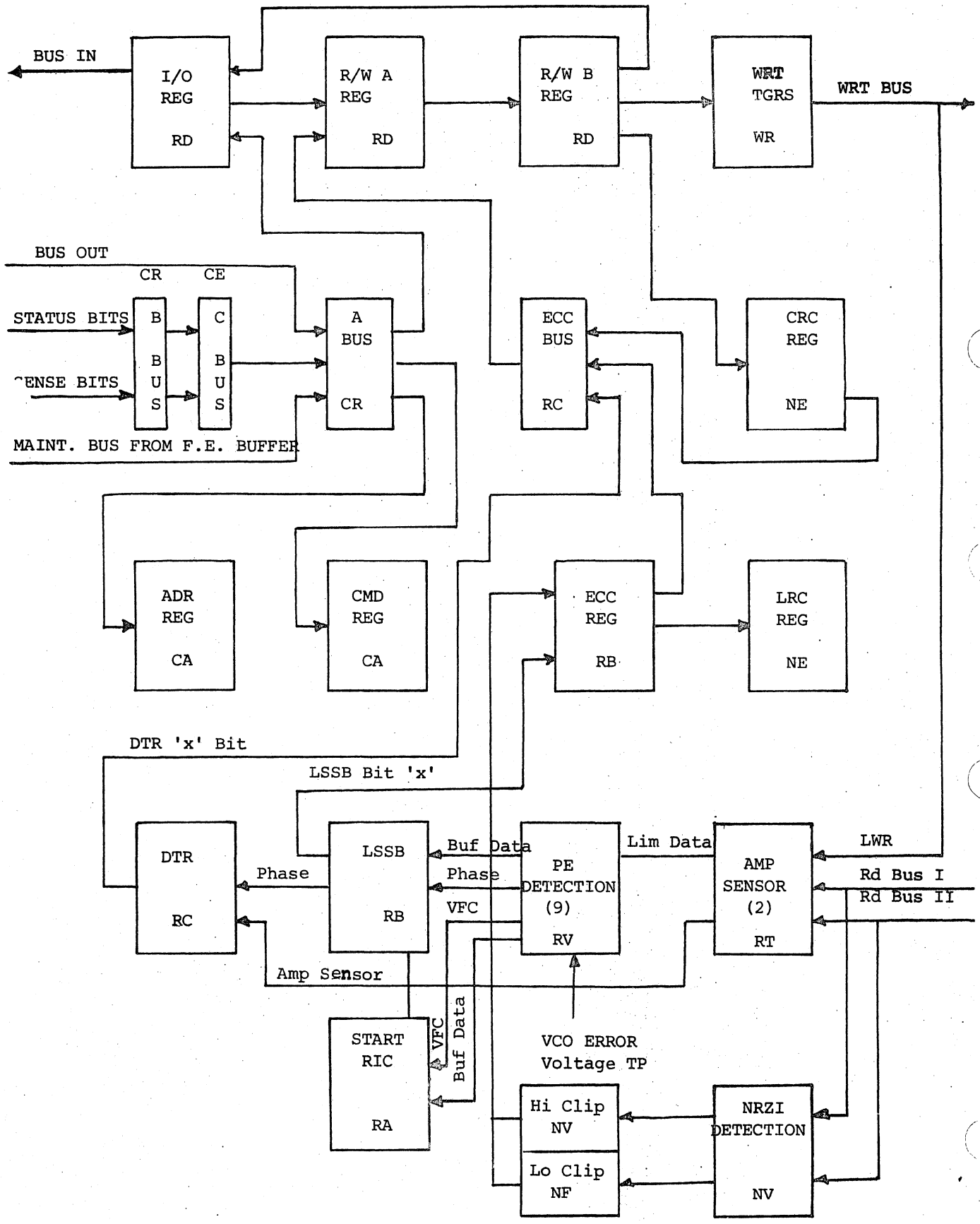

BUS IN
I/O REG
RD
R/W A REG
RD
R/W B REG
RD
WRT TGRS
WR
WRT BUS
BUS OUT
CR
CE
STATUS BITS
SENSE BITS
B BUS
C BUS
A BUS
CR
ECC BUS
RC
CRC REG
NE
MAINT. BUS FROM F.E. BUFFER
ADR REG
CA
CMD REG
CA
ECC REG
RB
LRC REG
NE
DTR 'x' Bit
LSSB Bit 'x'
DTR
RC
LSSB
RB
Buf Data
Phase
Phase
VFC
PE DETECTION (9)
RV
Lim Data
AMP SENSOR (2)
RT
LWR
Rd Bus I
Rd Bus II
Amp Sensor
START RIC
RA
VFC
Buf Data
VCO ERROR Voltage TP
Hi Clip
NV
Lo Clip
NF
NRZI DETECTION
NV

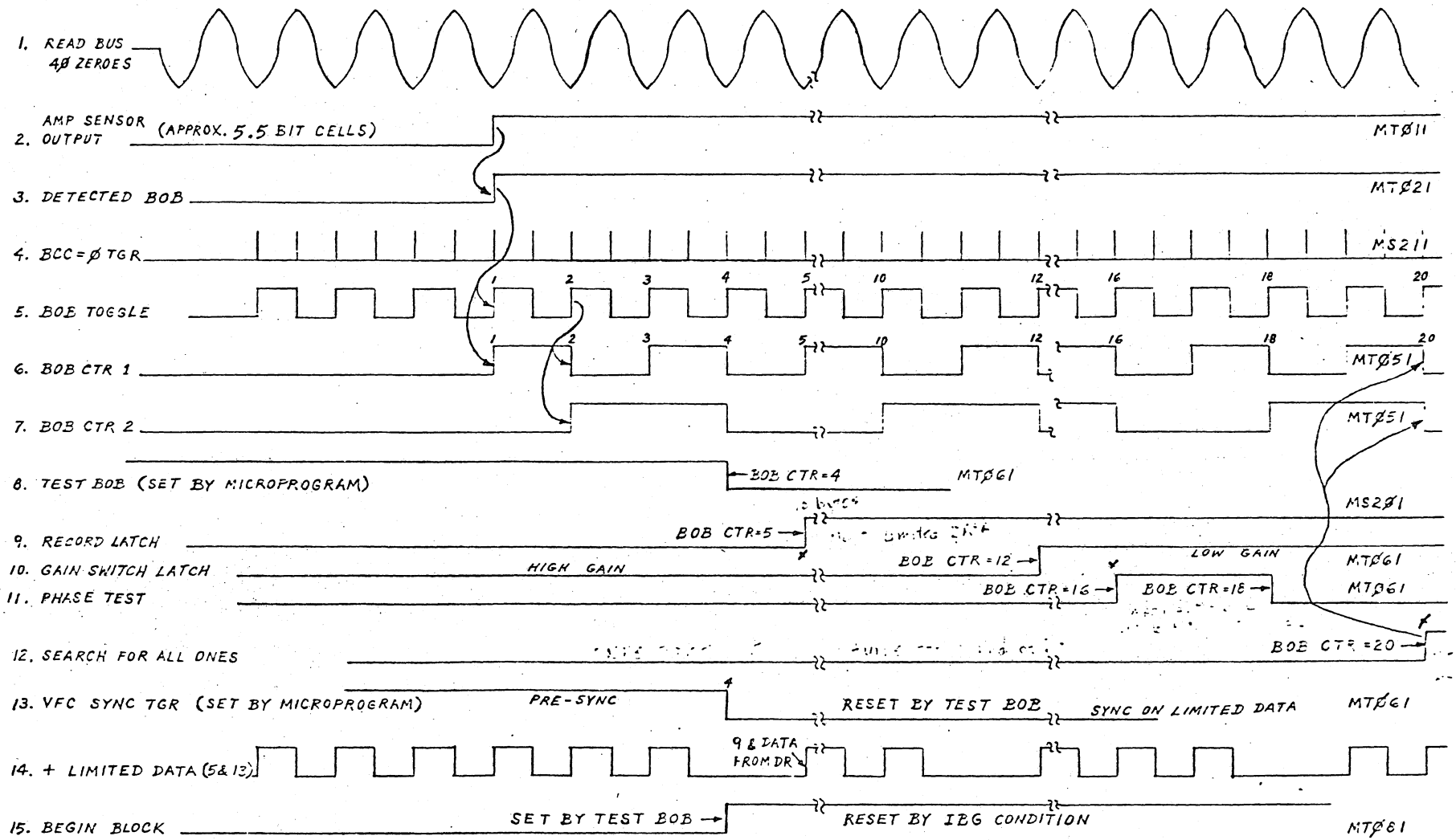


Figure 3-3. Read Detection, During 40 Zeroes.

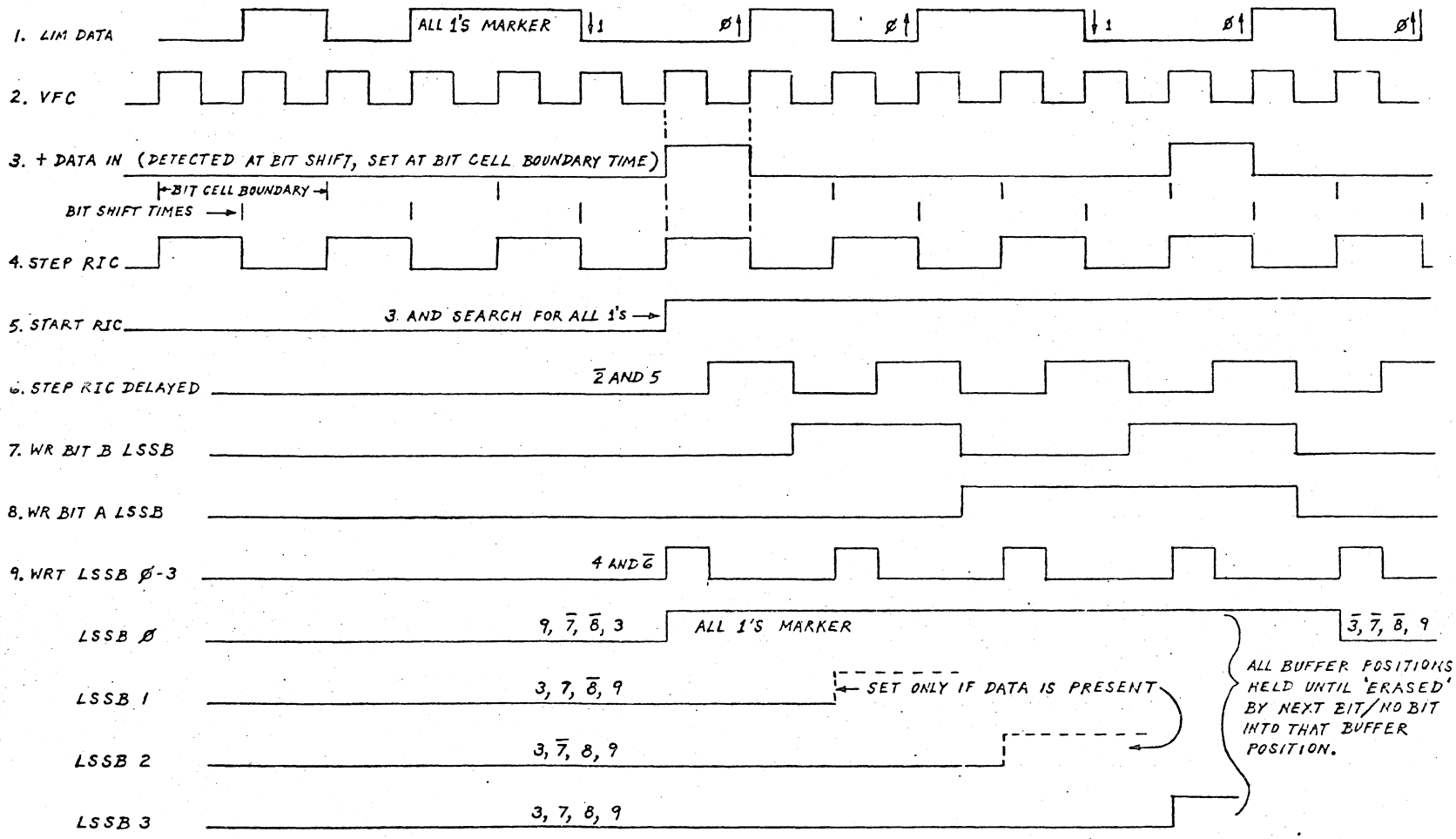


Figure 3-4. Read Detection, Data.

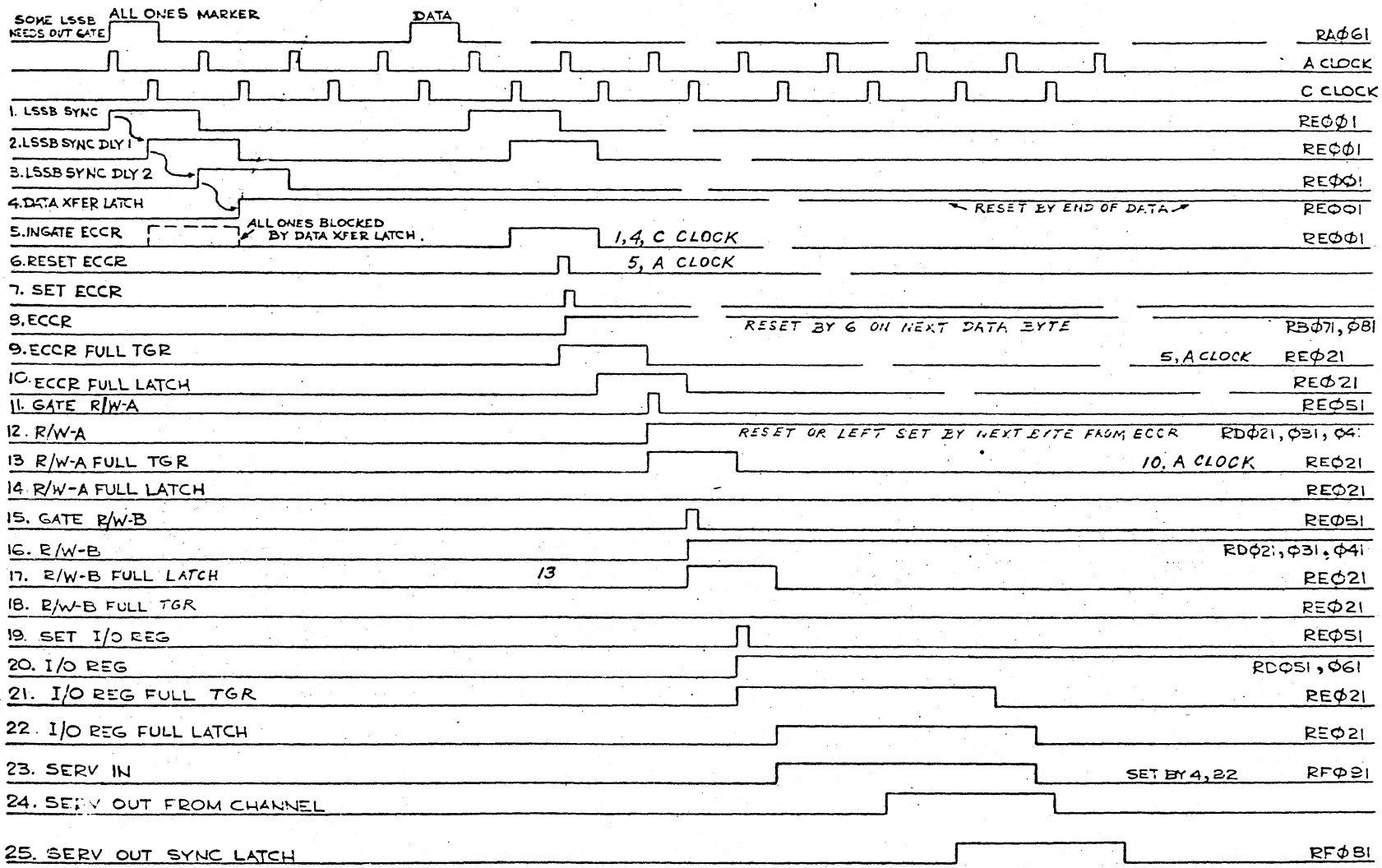


Figure 3-5. Read Data Transfer, Normal.

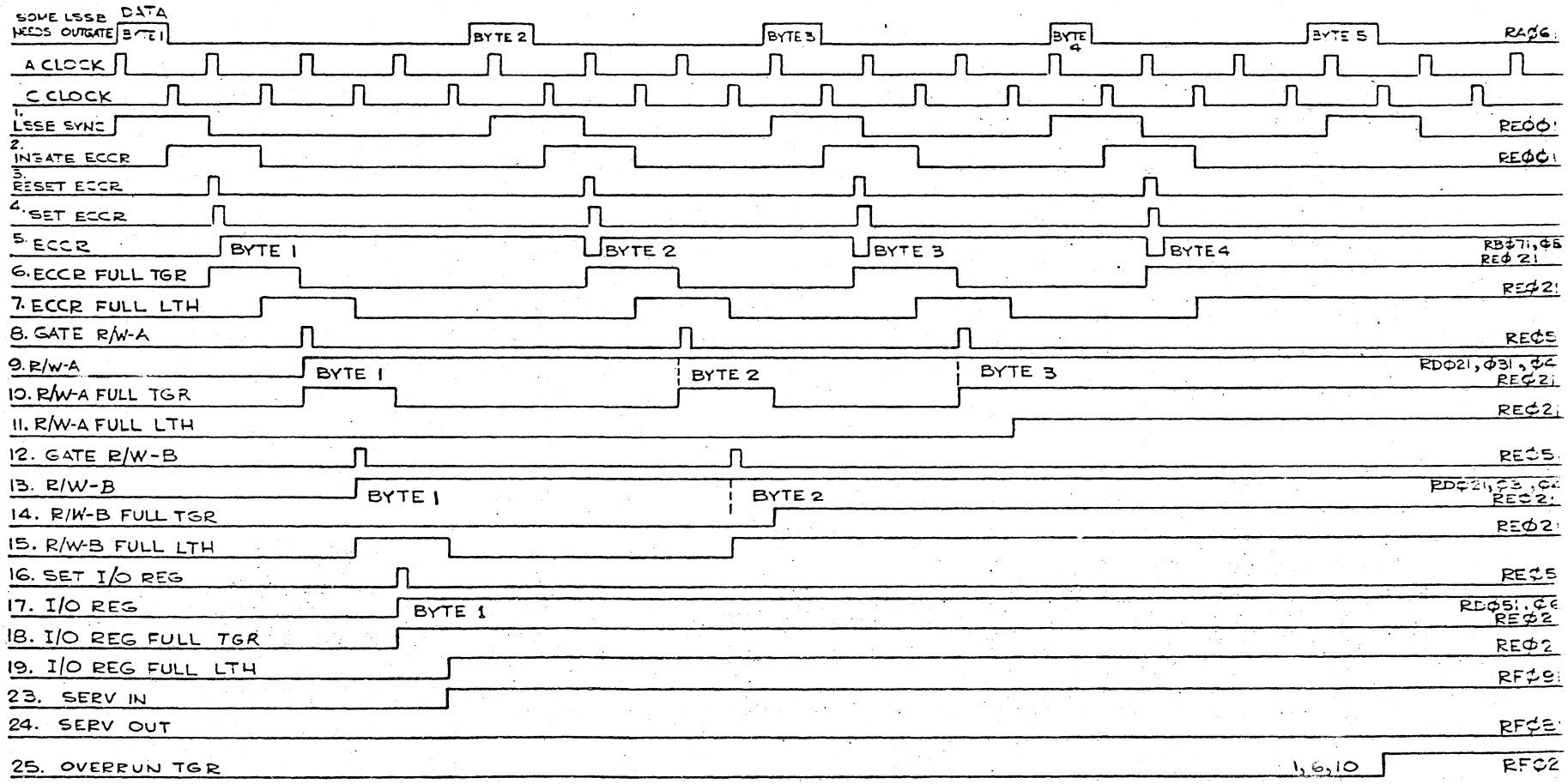
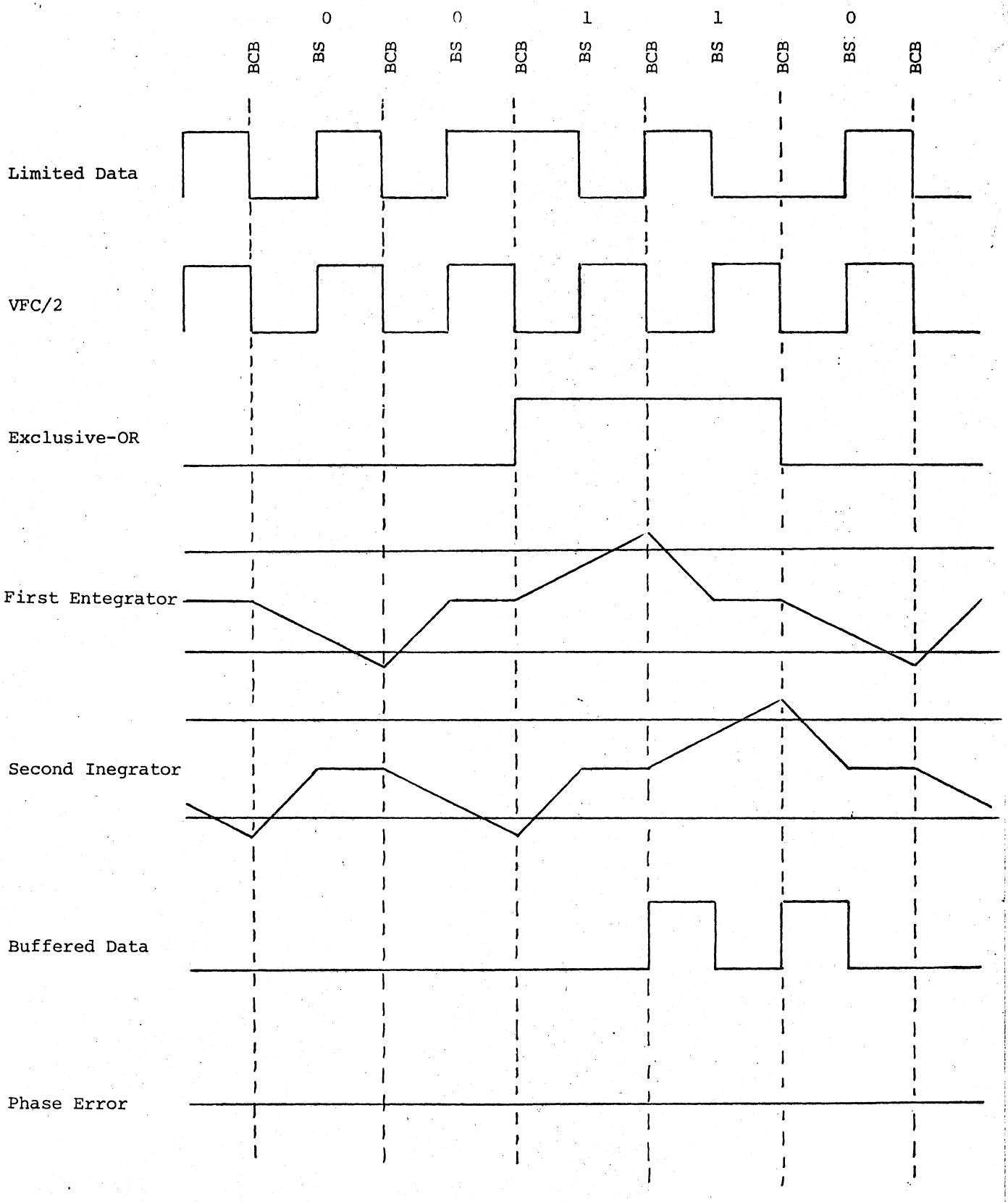
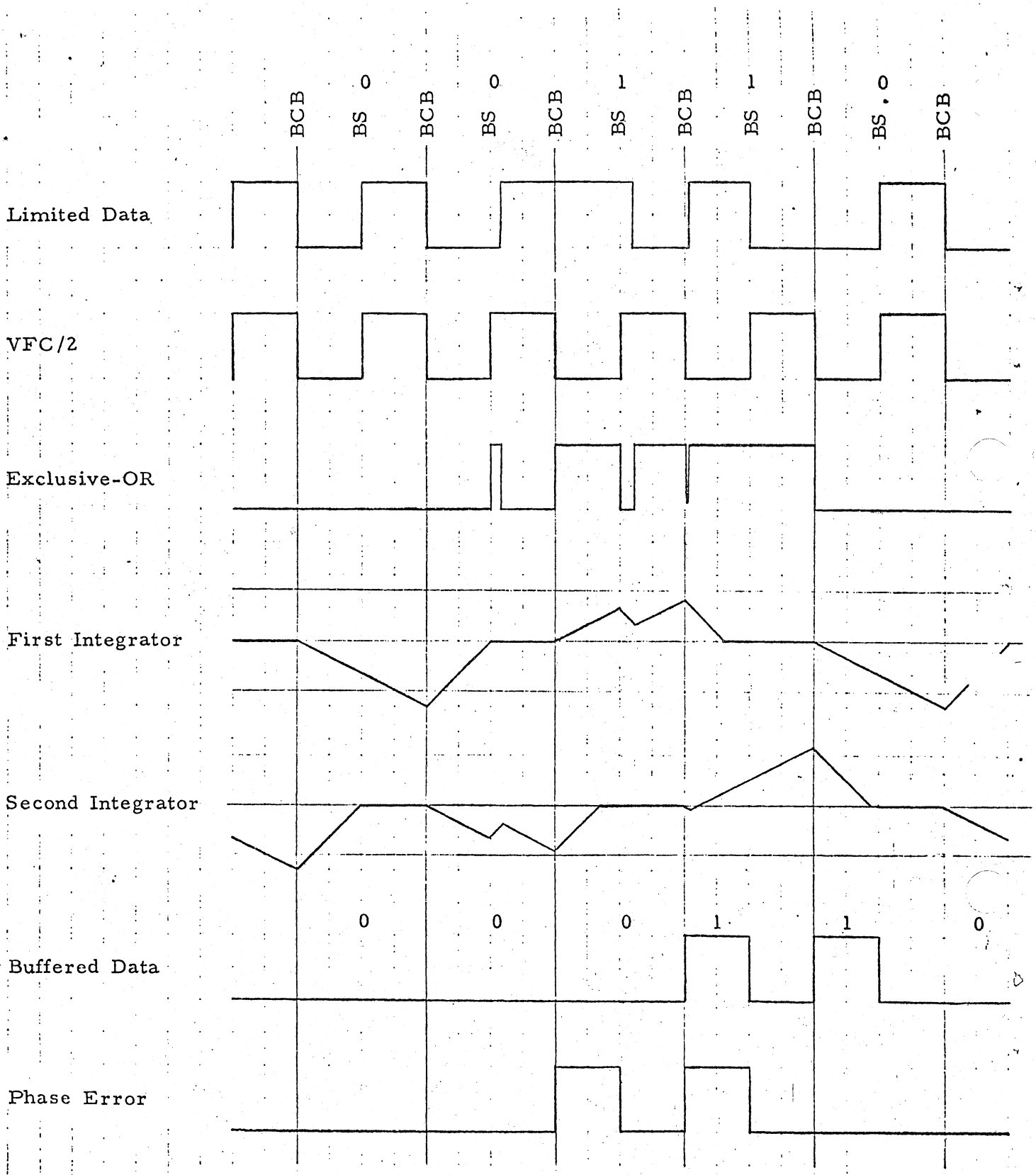


Figure 3-6. Read Overrun.


0
0
1
1
0
BCB
BS
BCB
BS
BCB
BS
BCB
BS
BCB
BS
BCB
Limited Data
VFC/2
Exclusive-OR
First Entegrator
Second Inegrator
Buffered Data
Phase Error


BCB
BS 0
BCB
BS 0
BCB
BS 1
BCB
BS 1
BCB
BS 0
BCB
Limited Data
VFC/2
Exclusive-OR
First Integrator
Second Integrator
0
0
0
1
1
0
Buffered Data
Phase Error